Compal Confidential

Intel M/B Schematics Document

Kabylake-U(2+2)-DDR4 SODIMMx2 (1.2mm_6L)

~~nVidia N16 gDDR5-2GB~~

~~(N16S-GTR : GM108-670/770: GeForce MX130)~~
~~(N16V-GMR1 : GM108-626/726:GeForce MX110)~~

Date :2018-01-08

Version :v0.3

Project : 2018OPP_Harry Potter(15.6")
EPK50 :LA-G07DP
(EPK52 :LA-G07EP=>v0.2 for PV)

~~(EPK50 :KBLU_4G:LA-G07AP)~~
~~(EPK50 :KBLU_2G:LA-G07AP)~~
~~(EPK50 :KBLU_4G:LA-G07BP)~~
(EPK50 :KBLU_2G:LA-G07AP)
(EPK52 :KBLR_4G:LA-G07BP)
(EPK52 :KBLR_2G:LA-G07CP)
DIS

(EPK50 :KBLU:LA-G07DP)
(EPK52 :KBLR:LA-G07EP)
UMA

(Modified&Ref from: 01."NFLC_KBLR_LAE802PR10_MV_FINAL")
(02."Canadiens_LA-F035P-R10_KBL-UR_2017-06-23_CPU")
(02."CNL-U ORB_DDX02_LA-F152PR01_0822B")

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2017/10/22

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Title	Cover Page	
Size	Document Number	Rev
Custom	LA-G07DP(KBL-U_UMA_6L)	v0.3
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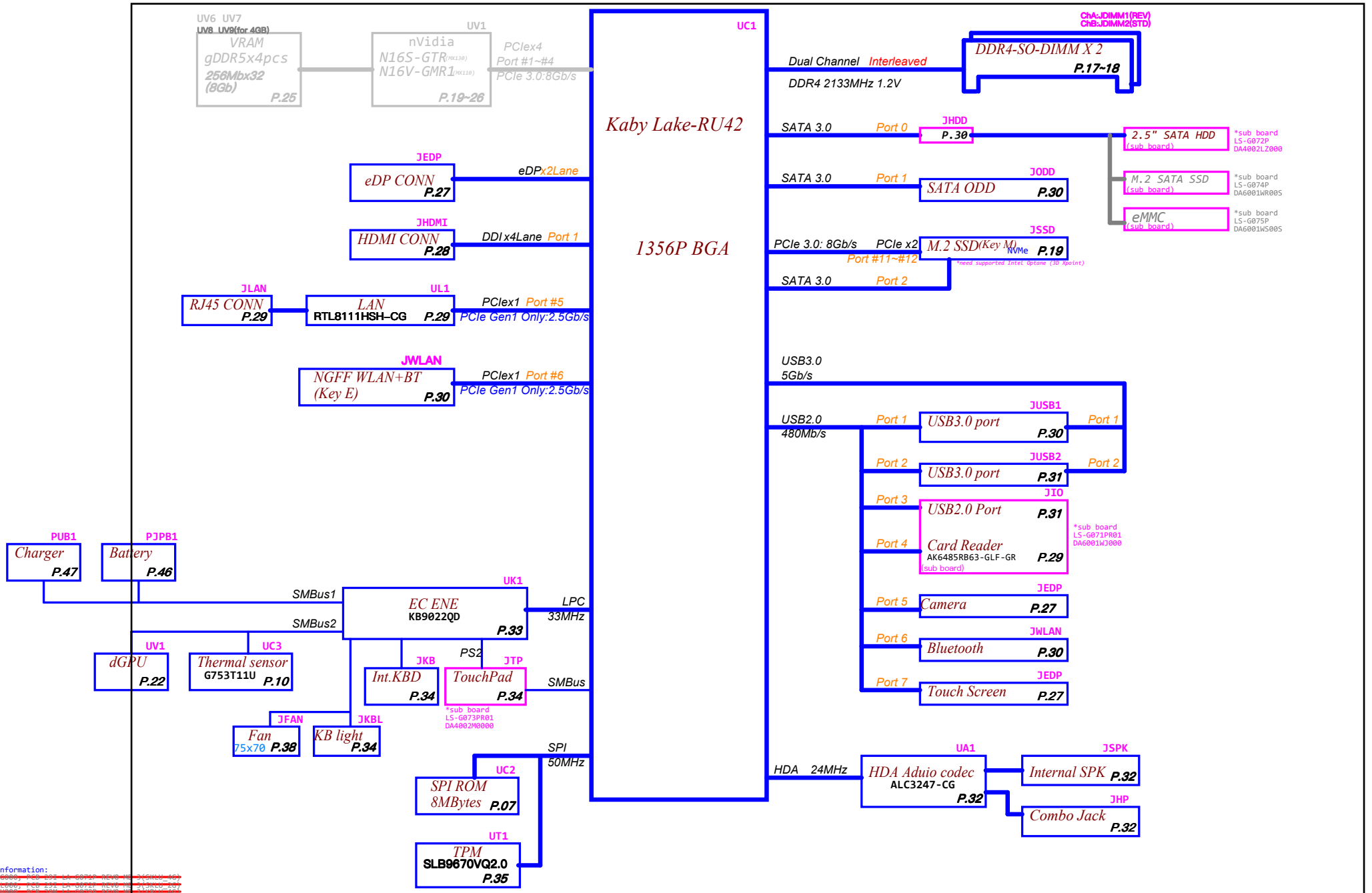

MB Board Information:

~~01.DA6001EC000, PCB 29K LA-G072P REV0 MB 3(KBLU_4G)~~
~~02.DA6001EM000, PCB 29M LA-G072P REV0 MB 3(KBLU_2G)~~
~~03.DA6001WL000, PCB 29L LA-G072P REV0 MB 3(KBLR_2G)~~
04.DA6001WM000, PCB 29M LA-G07AP REV0 MB 3(KBLU_2G)
05.DA8001EI000, PCB 29L LA-G07BP REV0 MB 3(KBLR_4G)
06.DA6001WI000, PCB 29L LA-G07CP REV0 MB 3(KBLR_2G)
07.DA6001YA000, PCB 29M LA-G07DP REV0 MB 3(KBLU_UMA)
08.DA6001YB000, PCB 29L LA-G07EP REV0 MB 3(KBLR_UMA)

Sub Board Information:(EPK52)
01.DA6001WJ000, PCB 29L LS-G071P REV0 IOB(4350M832L01)
02.DA4002LZ000, PCB 29L LS-G072P REV0 HDDB(4350M932L01)
03.DA4002M0000, PCB 29L LS-G073P REV0 TOUCH PADB(4350MA32L01)
04.DA6001WR00S, PCB 29L LS-G074P REV0 SSDB(4350MB32L01)
~~05.DA6001WS00S, PCB 29L LS-G075P REV0 SMSB~~

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

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Title: Block Diagrams

Size: Custom	Document Number: LA-G07DP(KBL-U_UMA_6L)	Rev: v0.3
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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBCLK SMBDATA	+3V_PRIM	DIMM1	0x50	0xA0	0xA1
		DIMM2	0x52	0xA4	0xA5
		Touch PAD	0x2C	0x58	0x59

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	
		Thermal Sensor	0x90
		PCH	

BOM Structure Table (1/2)

Function	Stuff	Un-Stuff
DGPU SKU	PX@	
UMA SKU	UMA@	
TPM	TPM@	

Power State

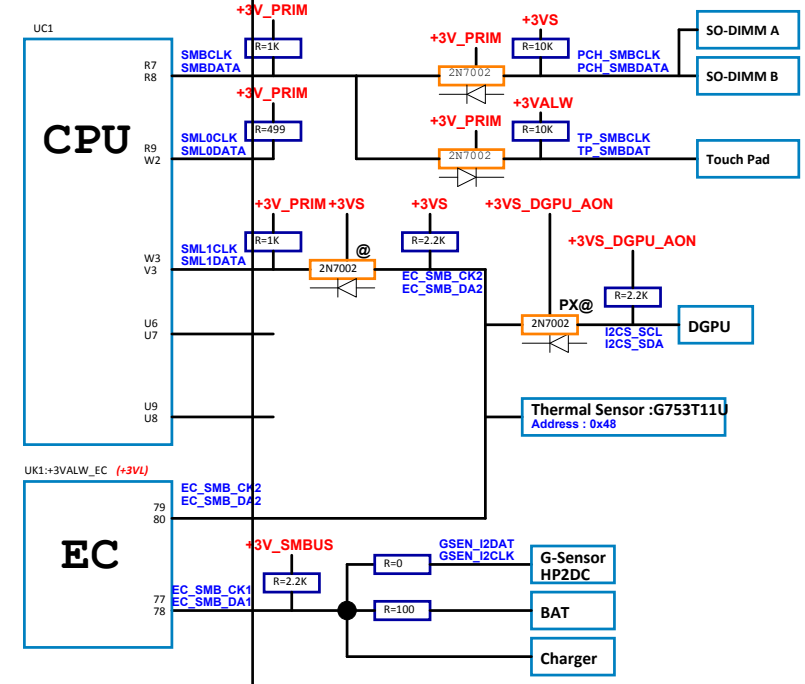
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

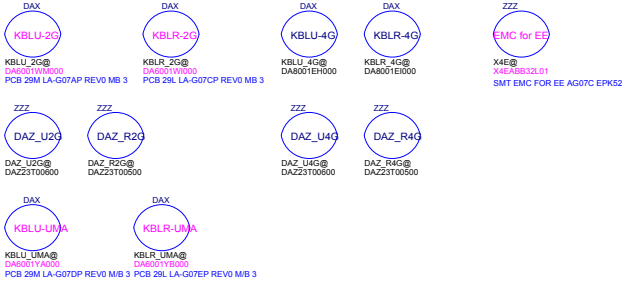
<USB2.0 port>

USB2.0 port	DESTINATION
1	USB3.0 Type-C
2	USB2.0/USB3.0
3	USB2.0/USB3.0
4	BT
5	HD/IR_1/IR_2 Camera
6	IR_2 Camera
7	Card Reader
8	X
9	X
10	X

<PCI-E,SATA,USB3.0/CLK>

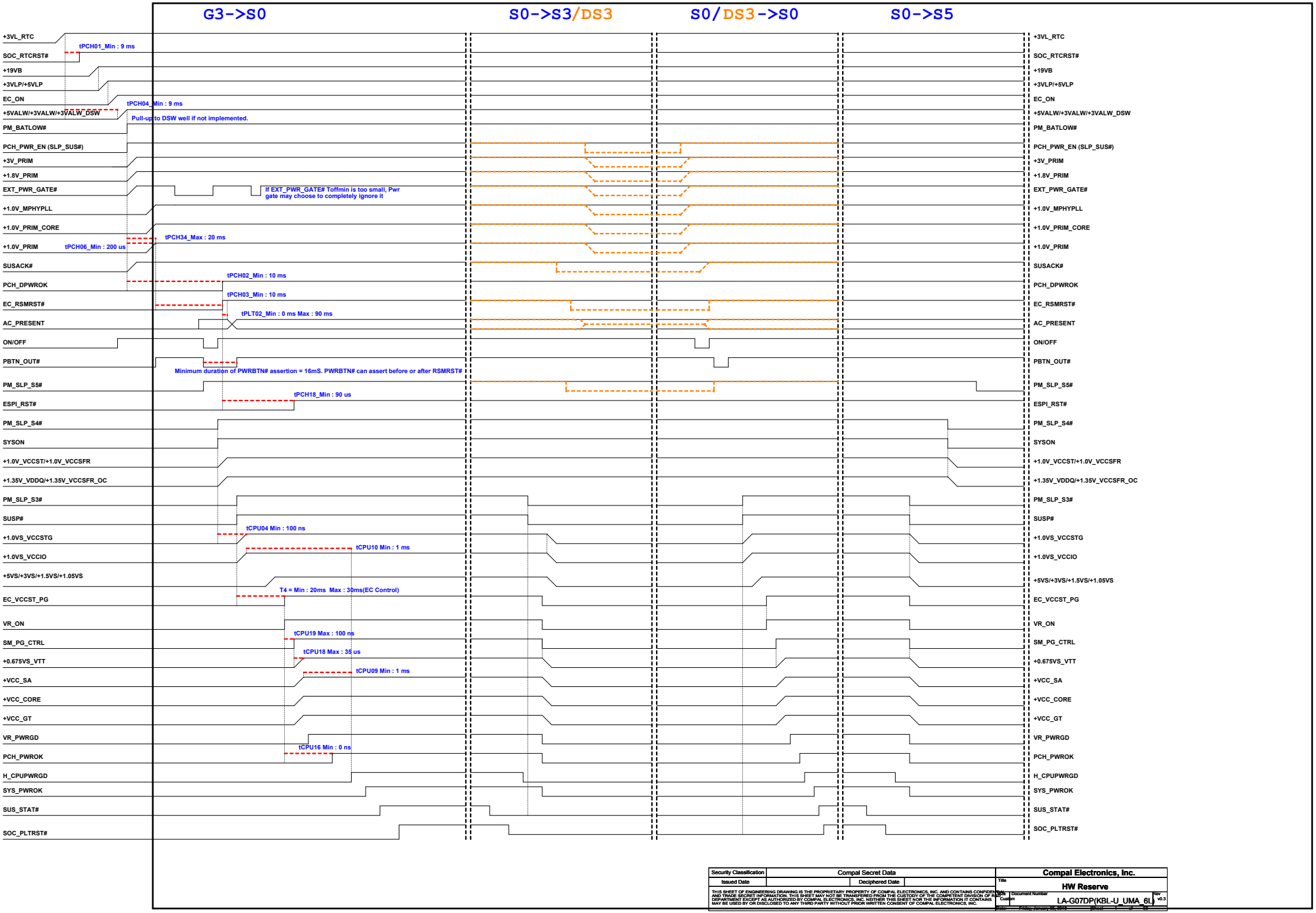
Lane#	PCI-E	SATA	USB3.0	DESTINATION		CLK
1			1	USB3.0 Type-C		X
2			2	USB3.0 Type-C		X
3			3	USB2.0/USB3.0		X
4			4	USB2.0/USB3.0		X
5	1		5	GPU(DIS only)		CLK0
6	2		6	GPU(DIS only)		
7	3			GPU(DIS only)		
8	4			GPU(DIS only)		
9	5			LAN		CLK1
10	6			WLAN		CLK2
11	7	0		HDD		X
12	8	1a		ODD		CLK3
13	9			X		X
14	10			X		X
15	11	1b*		NVMe x2	X	CLK4
16	12	2			SATA SSD	X





45@ ROYALTY HDMI W/LOGO
Part Number | Description
RO0000002HM | HDMI W/Logo:RO0000002HM
RO0000003HM

[Diner-PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]



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Issued Date		Deciphered Date	Title: HW Reserve

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Size	Document Number	Rev
Custom	LA-G07DP(KBL-U_UMA_6L)	v0.3
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SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

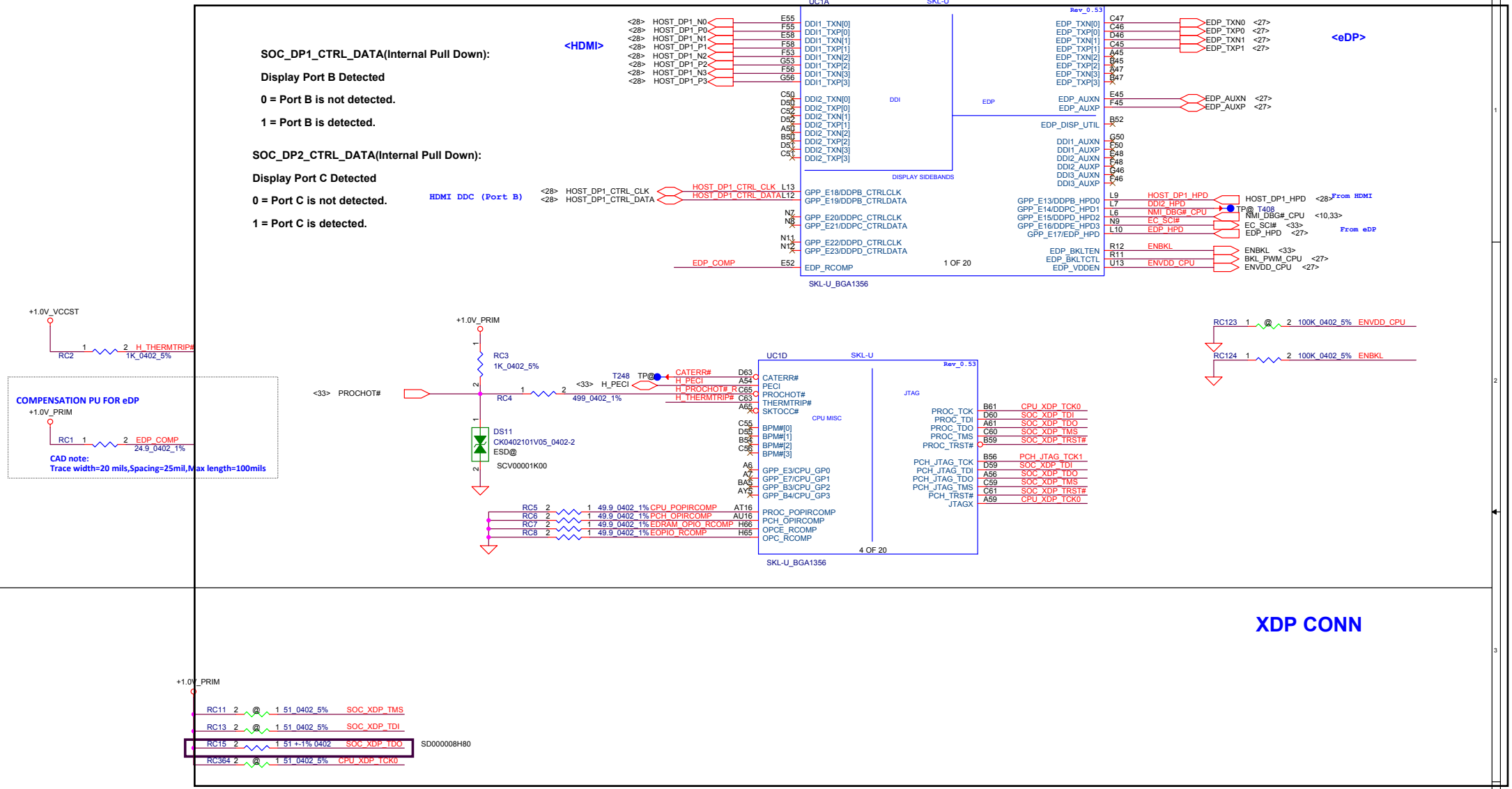
1 = Port B is detected.

SOC_DP2_CTRL_DATA(Internal Pull Down):

Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.



Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

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Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,MSIC,XDP,EDP

Size: Custom | Document Number: LA-G07DP(KBL-U_UMA_6L) | Rev: v0.3

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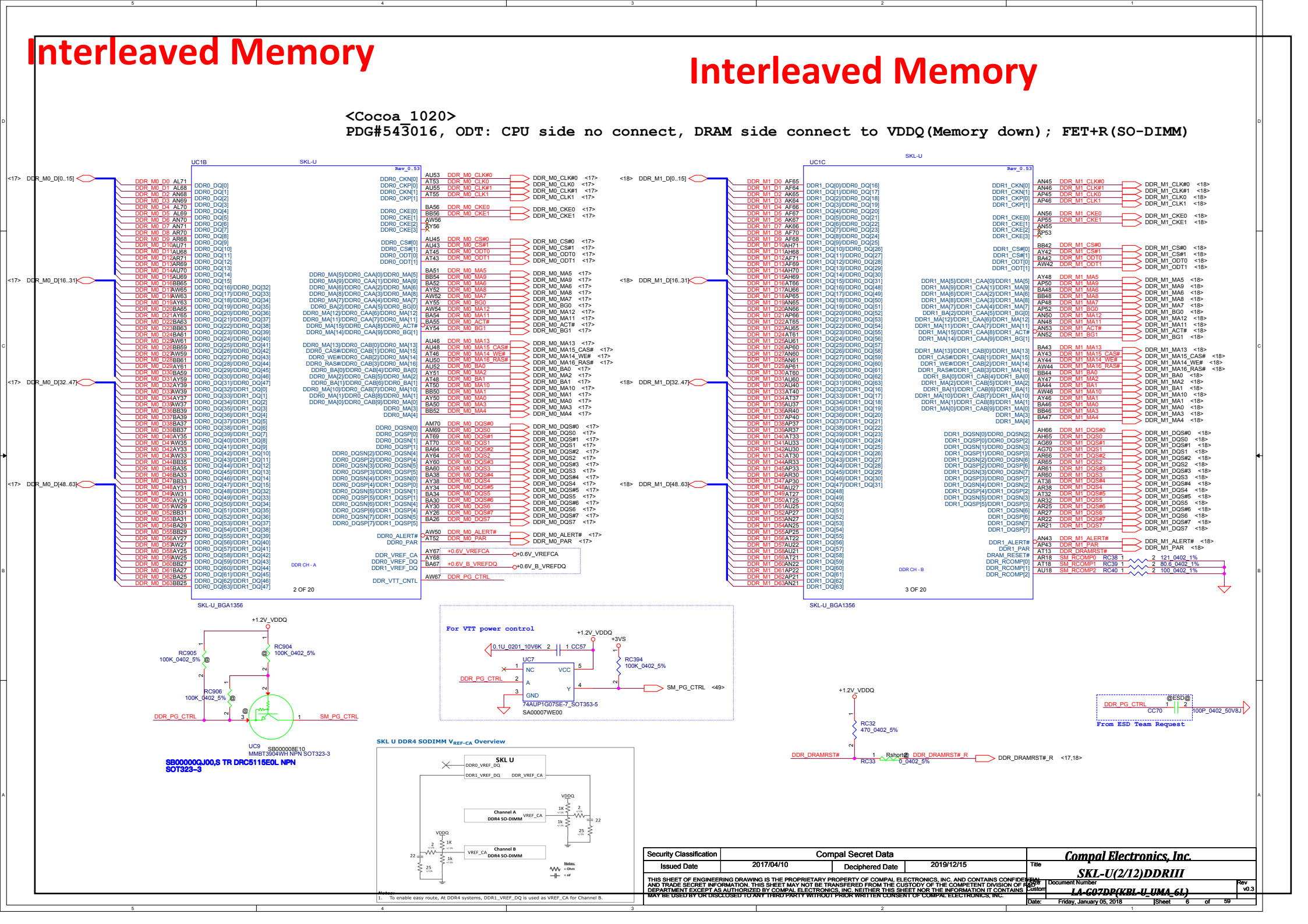
Interleaved Memory

Interleaved Memory

<Cocoa_1020>
PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down); FET+R(SO-DIMM)



Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

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Compal Electronics, Inc.			
Title	SKL-U(2/12)DDRIII		
Size	Document Number		Rev
Custom	LA-G07DP(KBL-U UMA 61)		v0.3
Date: Friday, January 05, 2018	Sheet 6 of 59		

SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

UC1E
SKL-U
Rev_0.53
SPI - FLASH
SMBUS, SMLINK
LPC
SPI - TOUCH
C LINK
5 OF 20
SKL-U_BGA1356

<35> HOST_SPI_0_SO
<35> HOST_SPI_0_SI
<35> HOST_SPI_0_CS2#
HOST_SPI_0_CLK AV2
HOST_SPI_0_SO AW3
HOST_SPI_0_SI AV3
HOST_SPI_0_SIO2 AW2
HOST_SPI_0_SIO3 AU4
HOST_SPI_0_CS0# AU3
AU2
HOST_SPI_0_CS2# AU1
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#

M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

G3 CL_CLK
G2 CL_DATA
G1 CL_RST#

<33> EC_KBRST#
To TPM <33,35> SERIRQ
LPC Mode
EC_KBRST# AW13
SERIRQ AY11
GPP_A0/RCIN#
GPP_A6/SERIRQ

GPP_C0/SMBCLK R7 SMBCLK
GPP_C1/SMBDATA R8 SMBDATA
GPP_C2/SMBALERT# R10 SMBALERT# TP@ T239
GPP_C3/SML0CLK R9 SML0CLK
GPP_C4/SML0DATA W2 SML0DATA
GPP_C5/SML0ALERT# W1 SML0ALERT#
GPP_C6/SML1CLK W3 SML1CLK
GPP_C7/SML1DATA V3 SML1DATA
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23 1 2 SML1ALERT#
RC902 @ 0_0201_5%
TP@ T234

GPP_A1/LAD0/ESPI_IO0 AY13 LPC_AD0 LPC_AD0 <33>
GPP_A2/LAD1/ESPI_IO1 BA13 LPC_AD1 LPC_AD1 <33>
GPP_A3/LAD2/ESPI_IO2 BB13 LPC_AD2 LPC_AD2 <33>
GPP_A4/LAD3/ESPI_IO3 AY12 LPC_AD3 LPC_AD3 <33>
GPP_A5/LFRAME#/ESPI_CS# BA12 LPC_FRAME# LPC_FRAME# <33>
GPP_A14/SUS_STAT#/ESPI_RESET# BA11 SUS_STAT# TP@ T2402

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 CLK_PCI0 RC387 1 2 22_0402_5% CLK_PCI_LPC <33> To EC
GPP_A10/CLKOUT_LPC1 AY9
GPP_A8/CLKRUN# AW11 PM_CLKRUN PM_CLKRUN# <33>
CC182 22P 50V J NPO 0402 EMI@

SMB
(Link to XDP, DDR, TP)
SML1
(Link to EC,DGPU, LAN, Thermal Sensor)

SML0ALERT# RC218 1K_0402_1%
+3V_PRIM
SML1ALERT# RC903 2 @ 1 150K_0402_1%
SML0ALERT# RC360 2 @ 1 10K_0402_5%
SMBALERT#
EC_KBRST#
RPC19 10K_0804_8P4R_5%
+3VS

to SPI ROM UC2 Source From

RPH11
HOST_SPI_0_CS0#_R 1 8 EC_SPI_CS0#
HOST_SPI_0_CS0#_R 2 7 HOST_SPI_0_CS0# EC_SPI_CS0# <33>
HOST_SPI_0_SO_R 3 6 EC_SPI_SO
HOST_SPI_0_SO_R 4 5 HOST_SPI_0_SO EC_SPI_SO <33>
15_0804_8P4R_5%

RPH12
HOST_SPI_0_HOLD# 1 8 HOST_SPI_0_SIO3
HOST_SPI_0_SI_R 2 7 HOST_SPI_0_SI
HOST_SPI_0_SI_R 3 6 EC_SPI_SI EC_SPI_SI <33>
4 5
15_0804_8P4R_5%

HOST_SPI_0_WP# 2 RC388 15_0402_5% 1 HOST_SPI_0_SIO2

SPI ROM (8MByte Only)
UC2
HOST_SPI_0_CS0#_R 1 CS# VCC 8 HOST_SPI_0_HOLD#
HOST_SPI_0_SO_R 2 DO(IO1) HOLD#(IO3) 7
HOST_SPI_0_WP# 3 WP#(IO2) CLK 6 HOST_SPI_0_CLK_R
4 GND DI(IO0) 5 HOST_SPI_0_SI_R
XM25QH64AHIG SOP 8P
SA0000B8300
ACES_91960-0084L_8P-T
Use socket footprint
SPI ROM Part:
Main:SA0000B8300, S IC FL 64M XM25QH64AHIG SOP 8P(XMC)
2nd: SA000039A40, S IC FL 64M W25Q64JVSSIQ SOIC 8P SPI ROM(Winbond)
3th: SA000085L00, S IC FL 64M MX25L6473FM2I-08G SOP 8P(MXIC)
+3V_SPI
CC8 1 2 0.1U_0201_10V6K

+3VS
RC216 10K_0402_5%
RC215 10K_0402_5%
QC1A
SMBCLK 6 1 PCH_SMBCLK <17,18>
L2N7002SDW1T1G 2N SC88-6
SB00001FF00
QC1B
SMBDATA 3 4 PCH_SMBDATA <17,18>
L2N7002SDW1T1G 2N SC88-6
SB00001FF00

+3V_PRIM
SML0CLK RC49 1 2 499_0402_1%
SML0DATA RC50 1 2 499_0402_1%
RPC7
SML1CLK 1 8
SML1DATA 2 7
SMBCLK 3 6
SMBDATA 4 5
1K_0804_8P4R_5%

+3VS
QC2A
SML1CLK 6 1 EC_SMB_CK2 <10,33>
L2N7002SDW1T1G 2N SC88-6
SB00001FF00
QC2B
SML1DATA 3 4 EC_SMB_DA2 <10,33>
L2N7002SDW1T1G 2N SC88-6
SB00001FF00
<DB> Un-pop QC2 for new 0x90 thermal sensor

+3V_SPI
HOST_SPI_0_SIO2 RC3901 @ 2 1K_0402_1%
HOST_SPI_0_SIO3 RC3911 @ 2 1K_0402_1%
HOST_SPI_0_CS0#_R 1 @ 2
RC357 1K_0402_5%

+3V_PRIM
+3VALW
RC81 10K_0402_5%
RC82 10K_0402_5%
SB00001FF00
QC7A
SMBCLK 1 6 TP_SMBCLK <34>
L2N7002SDW1T1G 2N SC88-6
QC7B SB00001FF00
SMBDATA 4 3 TP_SMBDATA <34>
L2N7002SDW1T1G 2N SC88-6

HOST_SPI_0_SIO3 RC51 1 ES@ 2 1K_0402_1%
From WW36 MOW for SKL-U ES sample

CLK Source CPU to SPI ROM UC2&EC
HOST_SPI_0_CLK 2 15_0402_5% 1 HOST_SPI_0_CLK_R
RC368 EMI@
HOST_SPI_0_CLK_R <33,35>
CC9 10P_0402_50V8J @EMI@

+3VS_PGPPA
PM_CLKRUN# RC107 1 2 8.2K_0402_5%
SERIRQ RC122 1 2 8.2K_0402_5%

Follow 543016_SKL_U_Y_PDG_0_9

EON SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P
MXIC SA00006N100 S IC FL 64M MX25L6473EM2I-10G SOP 8P
WINBOND SA000039A30 S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
Micron SA00005L100 S IC FL 64M N25Q064A13ESEC0F SO8W 8P

ENE Fixed Code Block Diagram
CPU
EC
SPI_ROM
M:Master
S : Slave
O : Output
I : Input

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Issued Date	2017/04/10	Deciphered Date	2019/12/15

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Compal Electronics, Inc.
Title: SKL-U(3/12)SPI,ESPI,SMB,LPC
Size: Custom
Document Number: LA-G07DP(KBL-U_UMA_6L)
Rev: v0.3
Date: Friday, January 05, 2018
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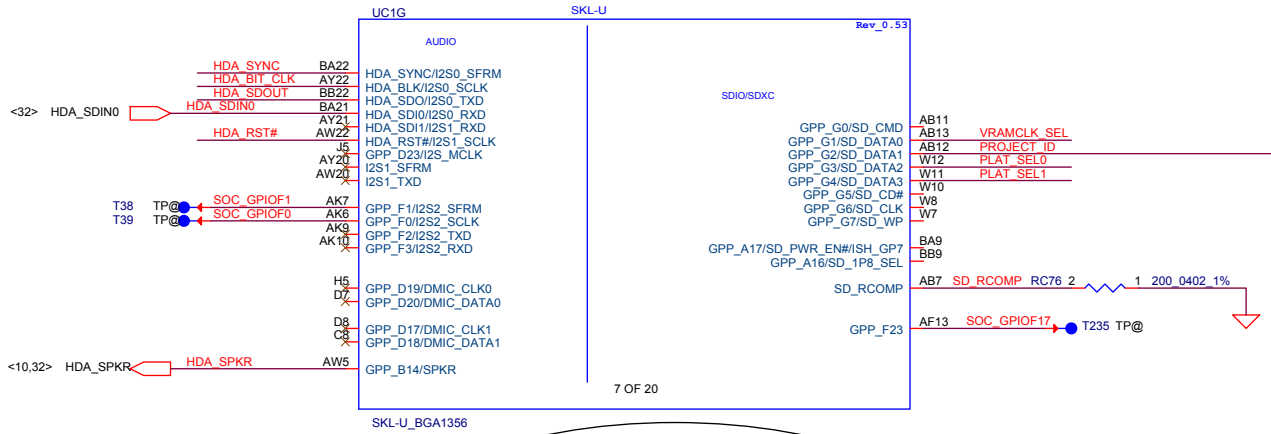
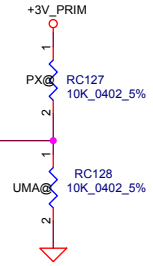
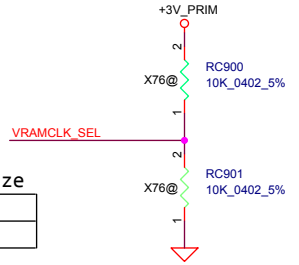




	UMA	DIS
PROJECT_ID	0	1

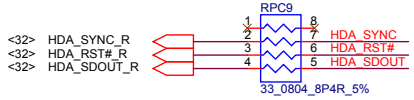
	2G VRAM	4G VRAM
VRAM Clock	0	1

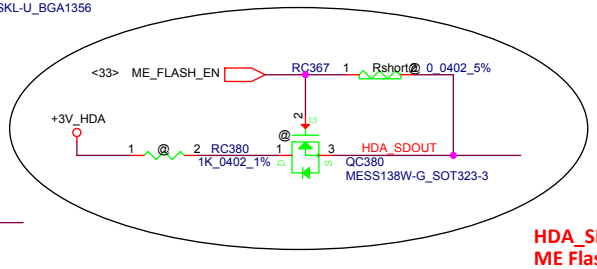


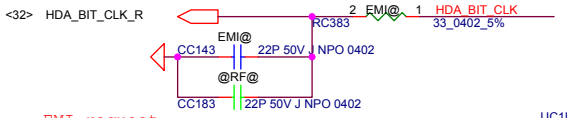
X76 BOM control RAM size

Net Name	4G	2G
VRAMCLK_SEL	1	0

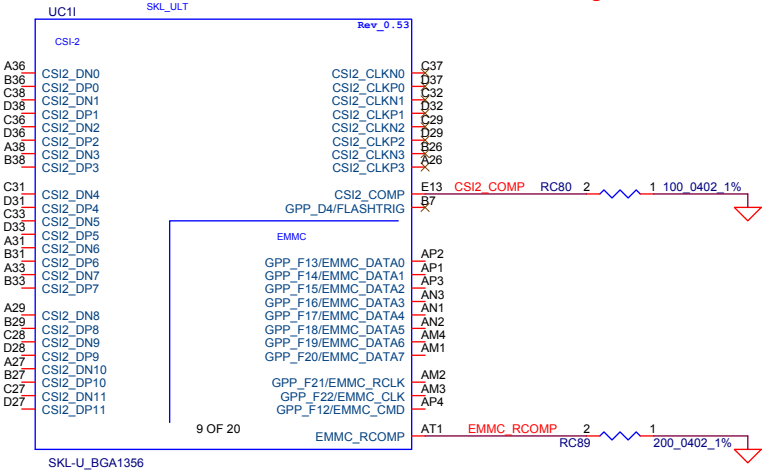
HDA for AUDIO

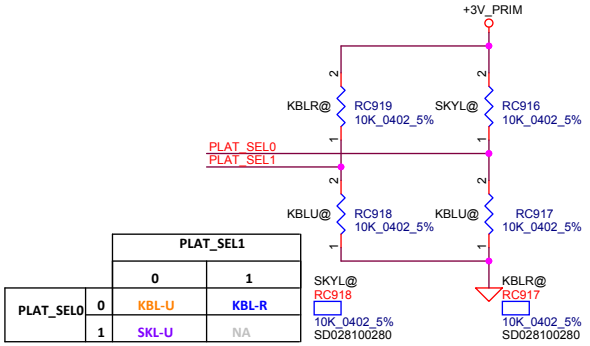






HDA_SDOUT:
ME Flash Descriptor Security Override
Low : Disabled(Default)
High : Enabled





PLAT_SEL0 \ PLAT_SEL1	0	1
0	KBL-U	KBL-R
1	SKL-U	NA

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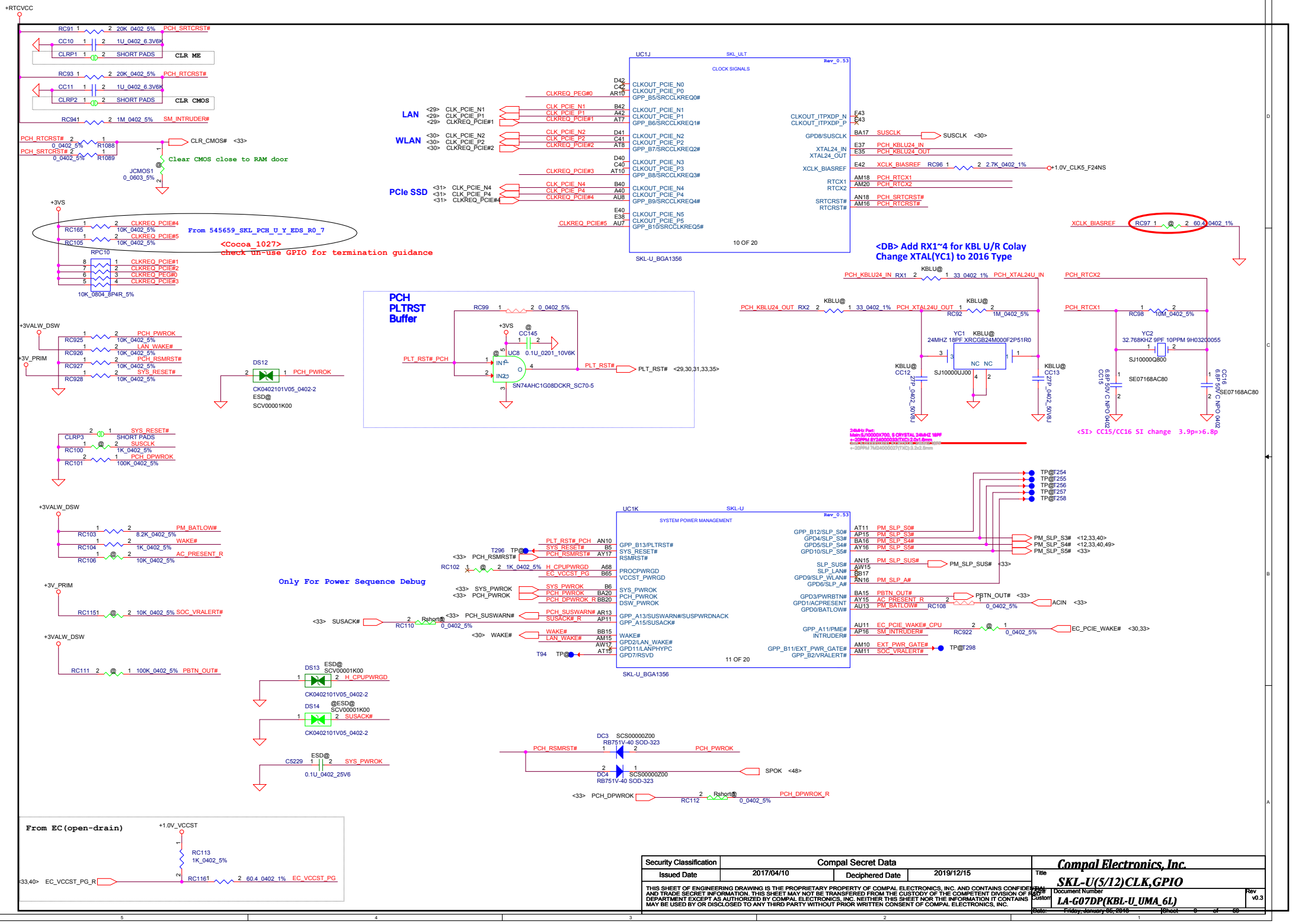
Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

Size: Custom | Document Number: LA-G07DP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 8 of 59



Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

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Compal Electronics, Inc.

Title: SKL-U(5/12)CLK,GPIO

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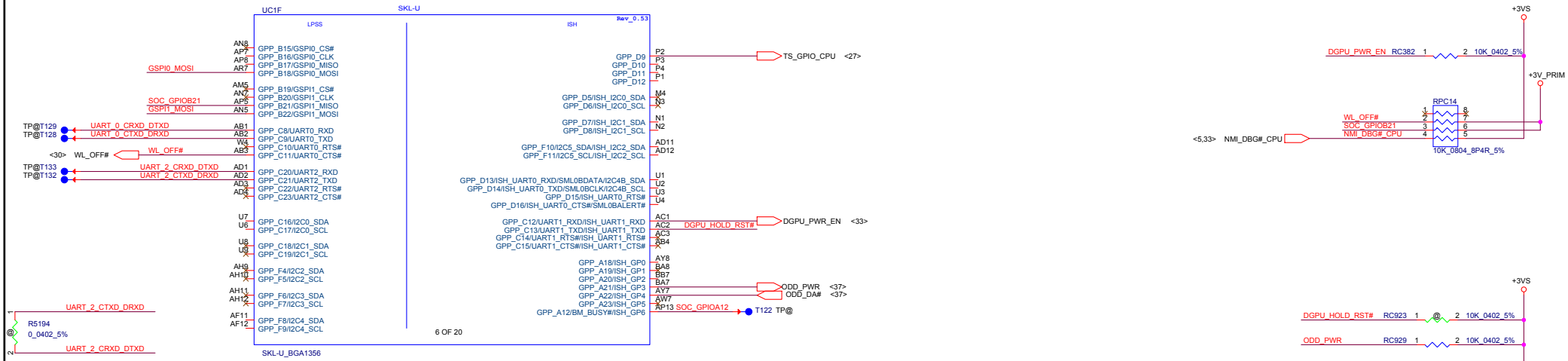
Date: Friday, January 05, 2018 | Sheet 9 of 59



Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.---> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

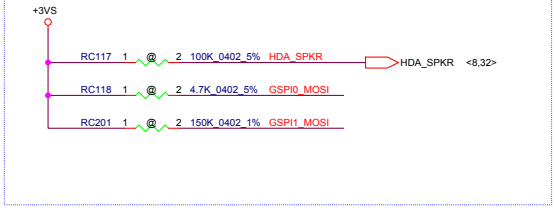
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

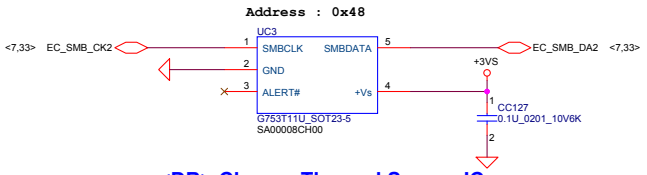
0 = SPI Mode --> AAX05 Use

1 = LPC Mode

Strap Pin



CPU THERMAL SENSOR



<DB> Change Thermal Sensor IC

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Title	SKL-U(6/12)GPIO		
Size: Custom	Document Number: LA-G07DP(KBL-U_UMA_6L)		Rev: v0.3
Date: Friday, January 05, 2018	Sheet 10 of 39		

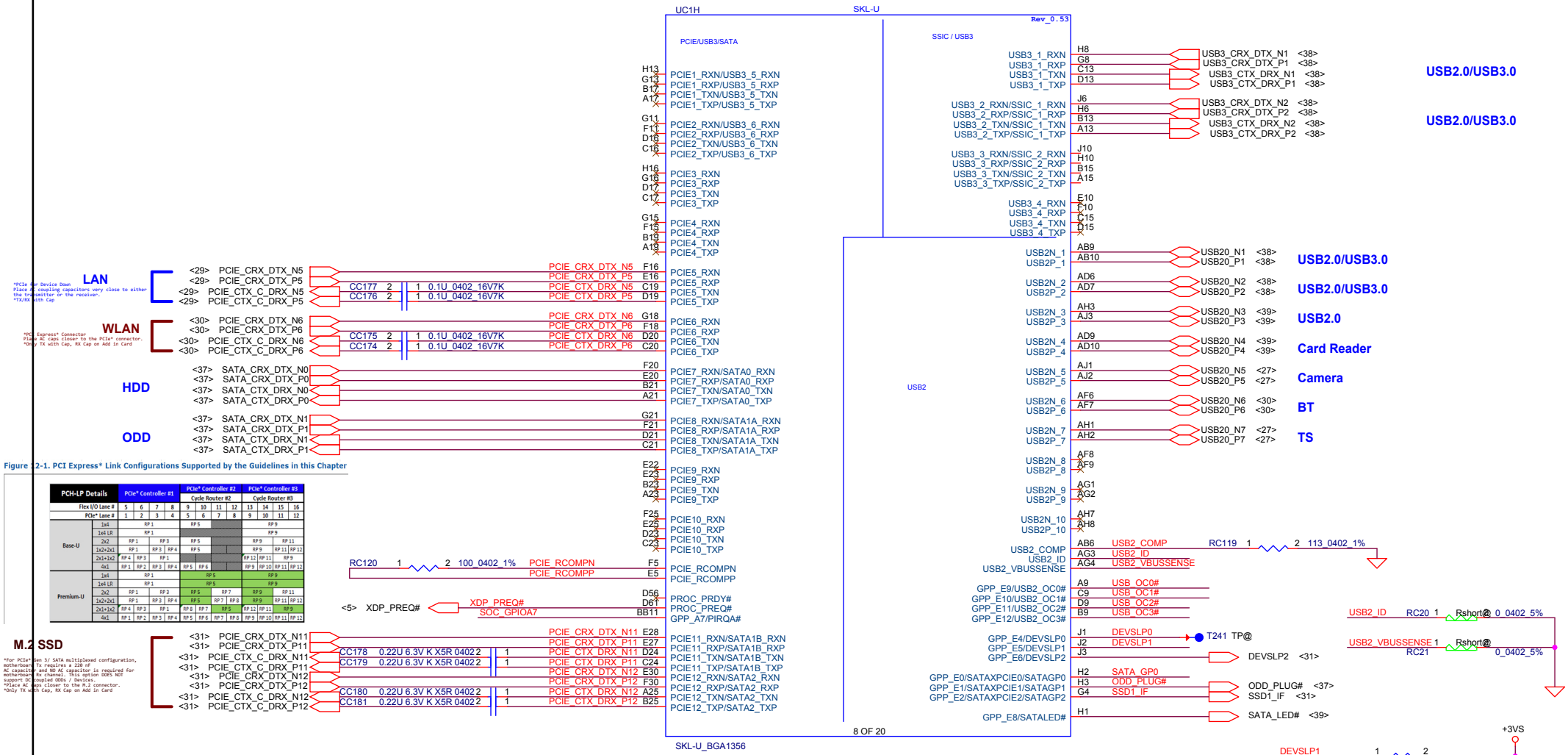
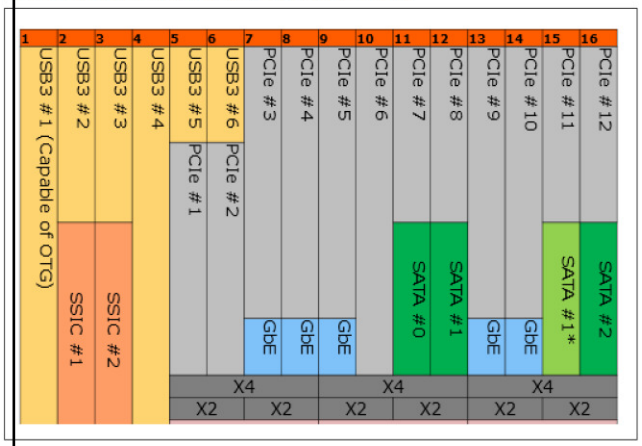


Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
						Cycle Router #2				Cycle Router #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1				RP 5				RP 9			
	1x4 LR	RP 1								RP 9			
	2x2	RP 1		RP 3		RP 5				RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1						RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6			RP 9	RP 10	RP 11	RP 12
Premium-U	1x4	RP 1				RP 5				RP 9			
	1x4 LR	RP 1				RP 5				RP 9			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12

High Speed I/O (HSIO) Lane Multiplexing in SKL U



When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1 and Port 2
USB_OC1#	USB2 Port 3
USB_OC2#	N/A
USB_OC3#	N/A
DEVSLP0	N/A
DEVSLP1	N/A
DEVSLP2	NGFF SSD KEY- M
SATA_GP0	N/A
SATA_GP1	ODD_PLUG#
SATA_GP2	PCIE/SATA

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Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

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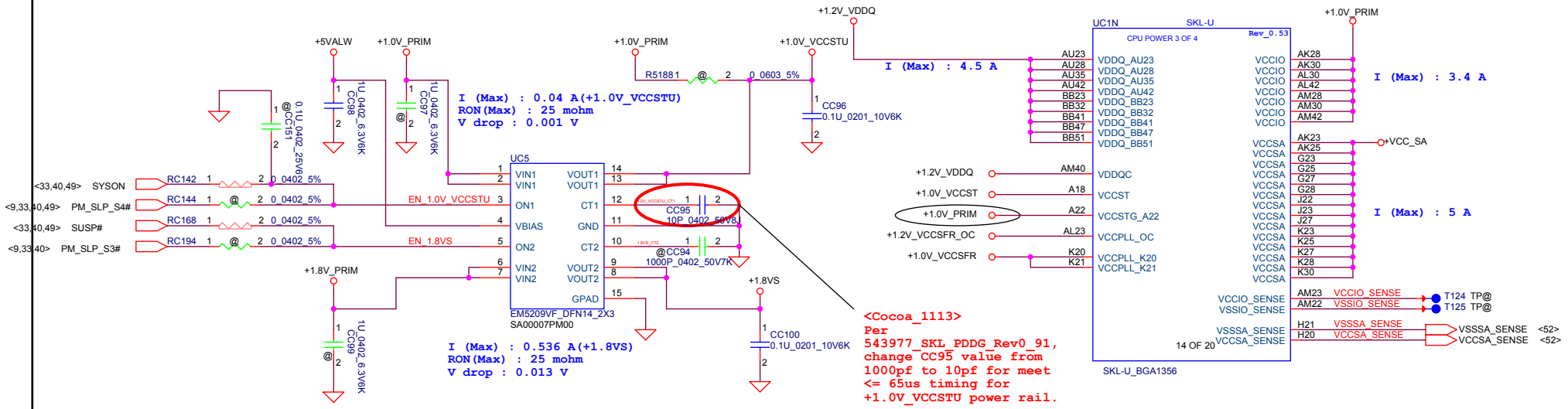
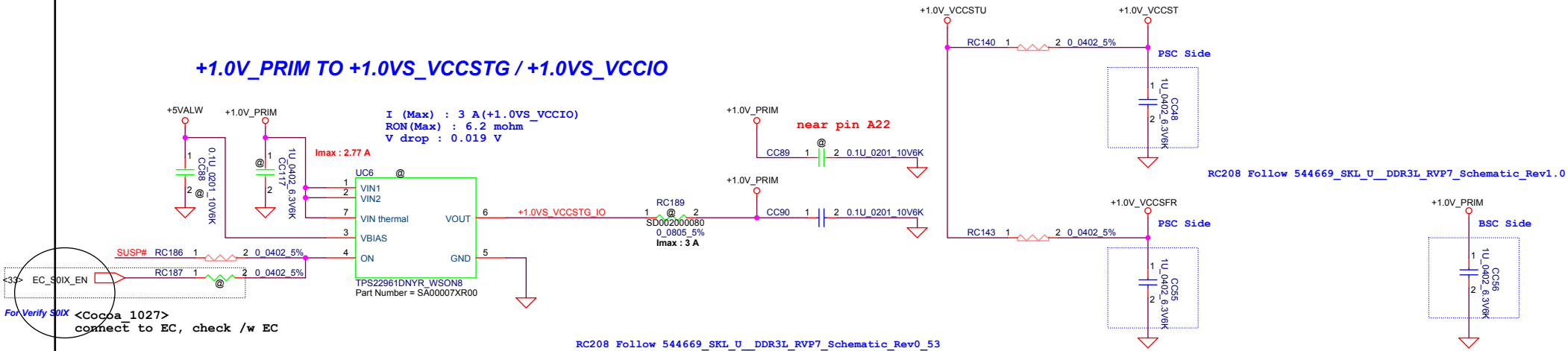
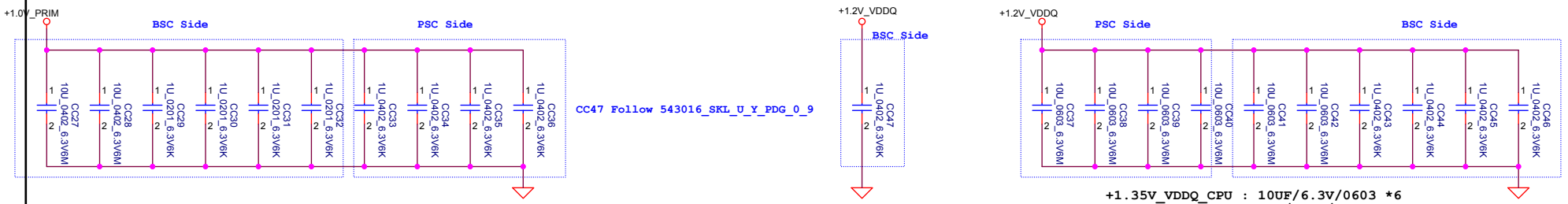
Date: Friday, January 05, 2018 | Sheet 11 of 59

+1.0V_PRIM TO +1.0V_VCCSTU



+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO





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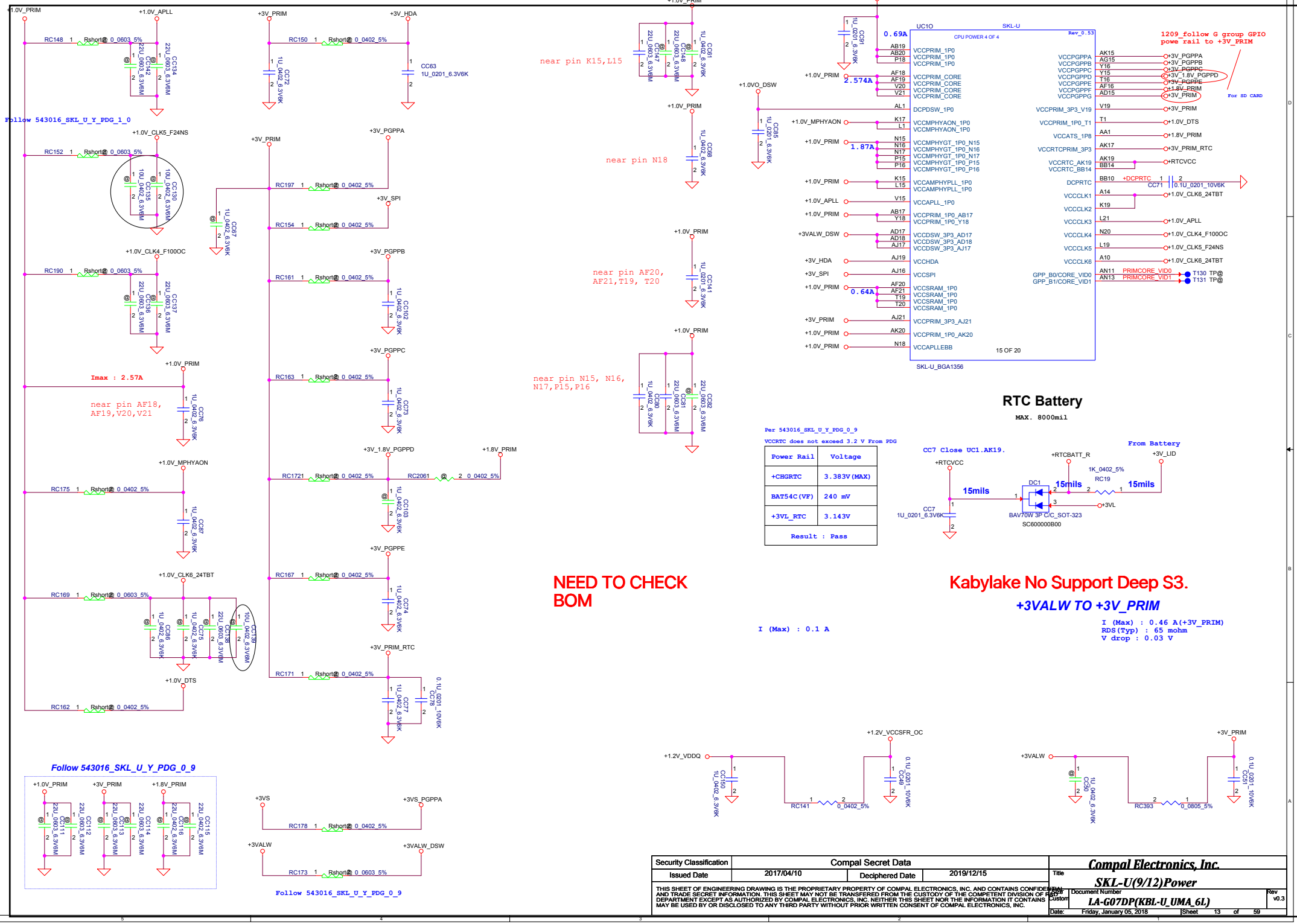
Size: Custom	Document Number: LA-G07DP(KBL-U_UMA_6L)		Rev: v0.3
Date: Friday, January 05, 2018	Sheet 12 of 59		



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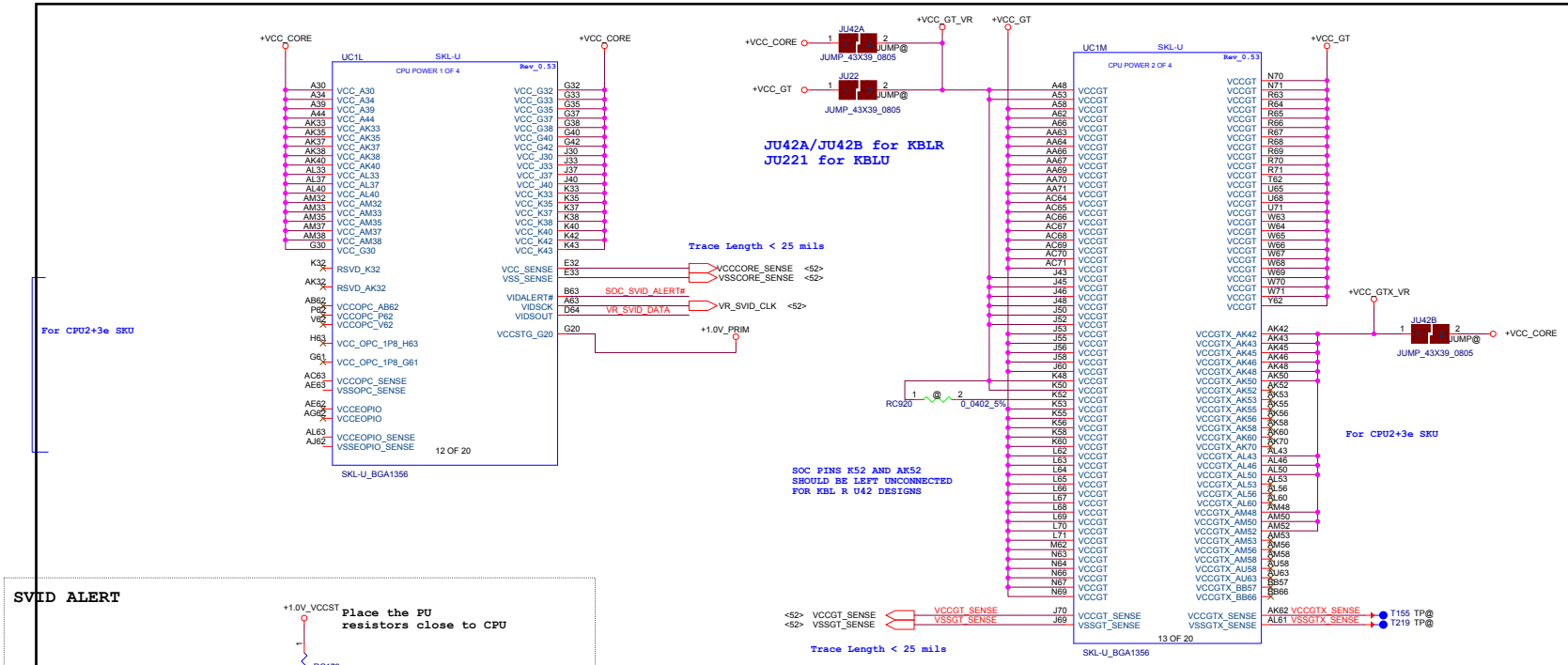
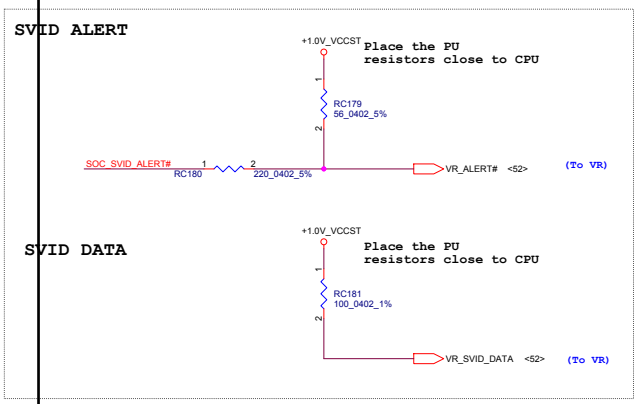
Compal Electronics, Inc.

Title: SKL-U(9/12)Power

Size: Custom | Document Number: LA-G07DP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 13 of 59





Ball #	Ball Names R-U42	Ball Names U22	R-U42/U22 common board guidelines
C7	XTAL24_OUT	NC	connect to R-U42 XTAL24_OUT
E3	XTAL24_IN	NC	connect to R-U42 XTAL24_IN
E35	NC	XTAL24_OUT	connect to U22 XTAL24_OUT
E37	NC	XTAL24_IN	connect to U22 XTAL24_IN
AK42	VCCCORE	VccGTx	
AK43	VCCCORE	VccGTx	
AK45	VCCCORE	VccGTx	
AK46	VCCCORE	VccGTx	
AK48	VCCCORE	VccGTx	
AK50	VCCCORE	VccGTx	connect to VccGTx/VCCCORE
AL43	VCCCORE	VccGTx	power plane island
AL46	VCCCORE	VccGTx	
AL50	VCCCORE	VccGTx	
AM48	VCCCORE	VccGTx	
AM50	VCCCORE	VccGTx	
AM52	VCCCORE	VccGTx	
J43	VCCCORE	VCCGT	
J45	VCCCORE	VCCGT	
J46	VCCCORE	VCCGT	
J48	VCCCORE	VCCGT	
J50	VCCCORE	VCCGT	connect to VccGT/VCCCORE
J52	VCCCORE	VCCGT	power plane island
K48	VCCCORE	VCCGT	
K50	VCCCORE	VCCGT	
A48	VCCCORE	VCCGT	
A53	VCCCORE	VCCGT	
AK52	RSVD	VccGTx	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.
K52	RSVD	VCCGT	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.

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Size: Custom	Document Number: LA-G07DP(KBL-U_UMA_6L)		Rev: v0.3
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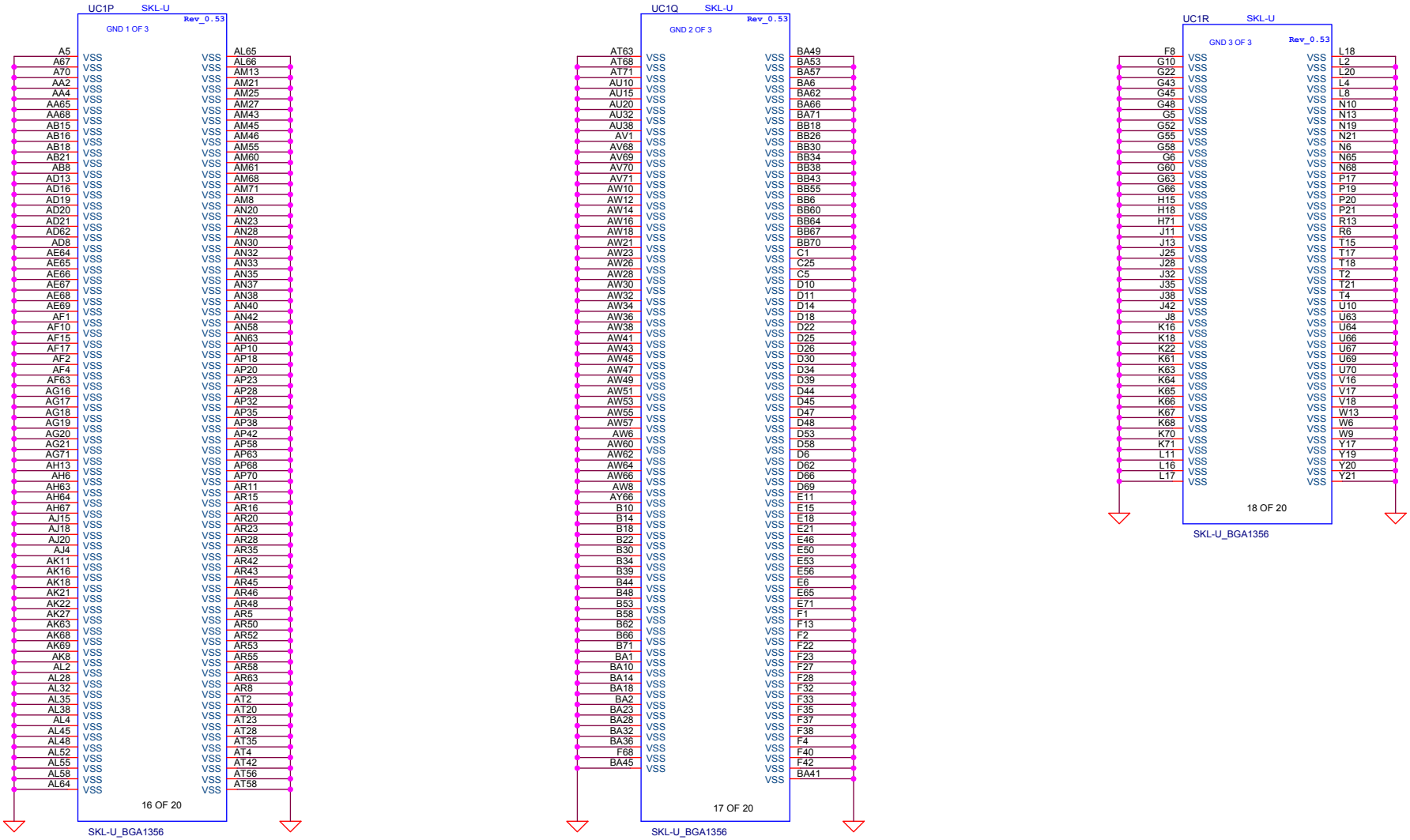

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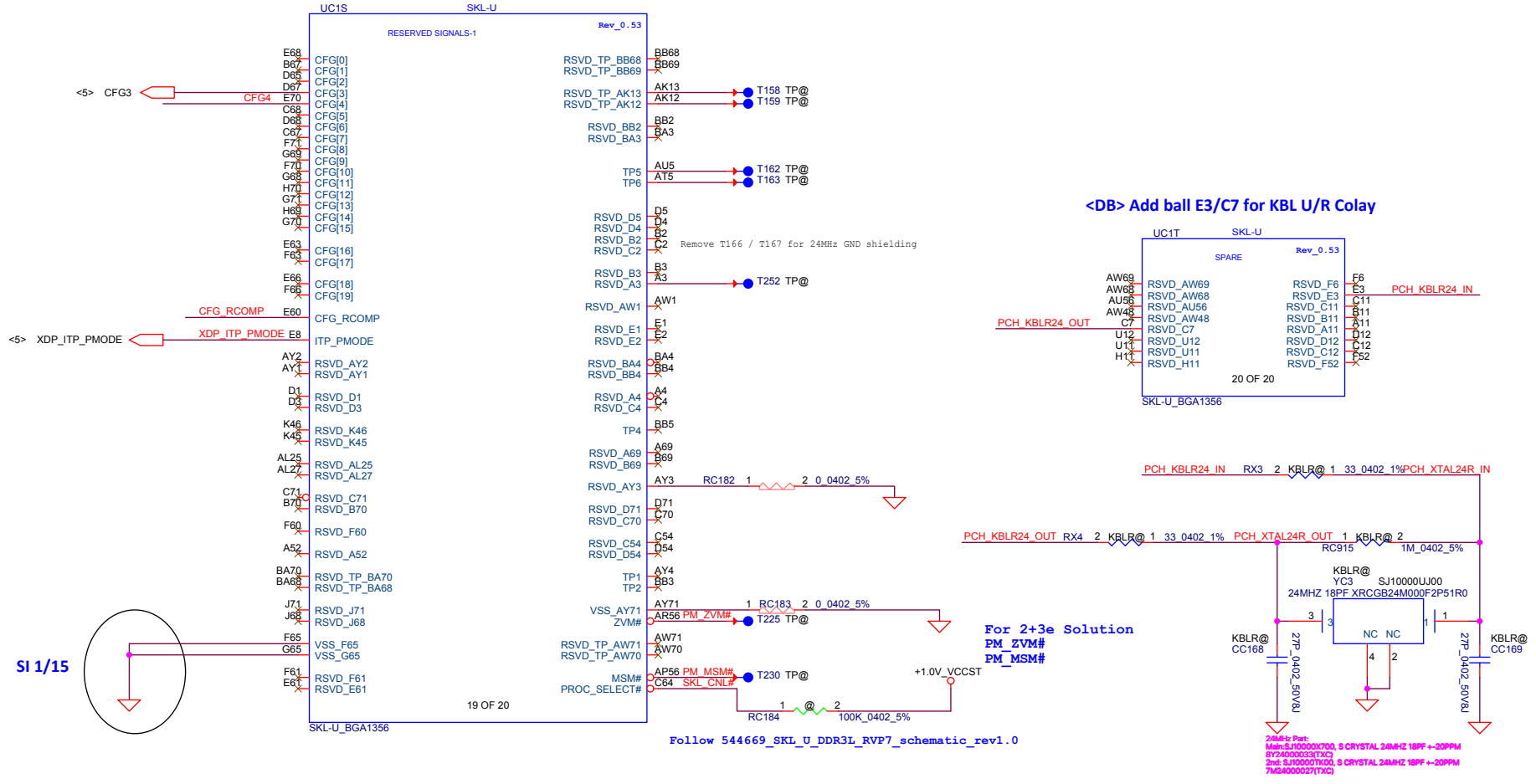
Title: **SKL-U(11/12)GND**

Size: Custom | Document Number: **LA-G07DP(KBL-U_UMA_6L)** | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 15 of 59



For 2+3e Solution
PM_ZVM#
PM_MSM#

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Title: SKL-U(12/12)RSVD

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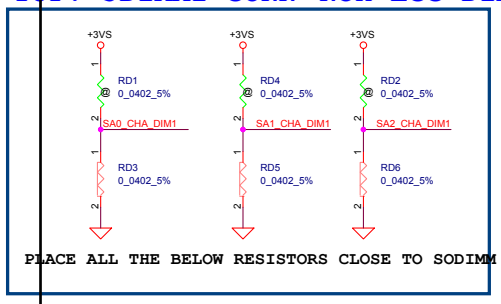
Date: Friday, January 05, 2018 | Sheet 16 of 59

CHANNEL-A

REVERSE TYPE

Interleaved Memory

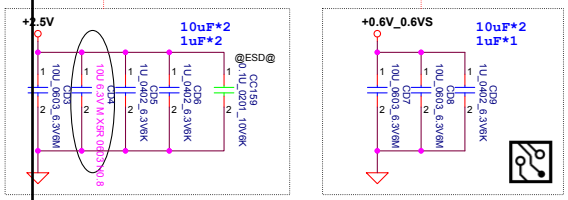
TOP: JDIMM1 CONN Non-ECC DIMM



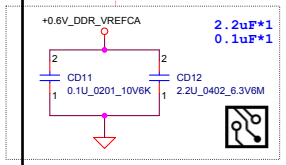
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258



Layout Note:
PLACE THE CAP near JDIMM1. 164



Layout Note:
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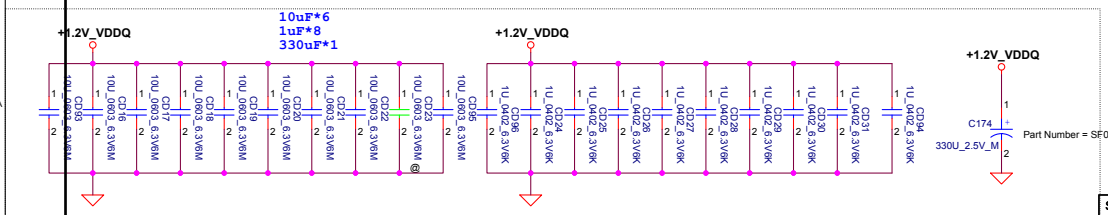
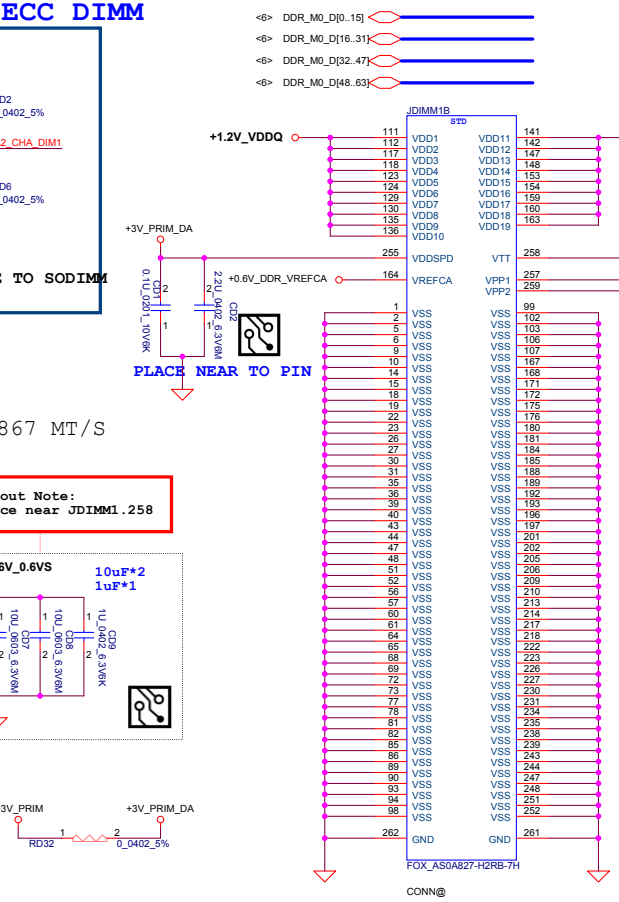
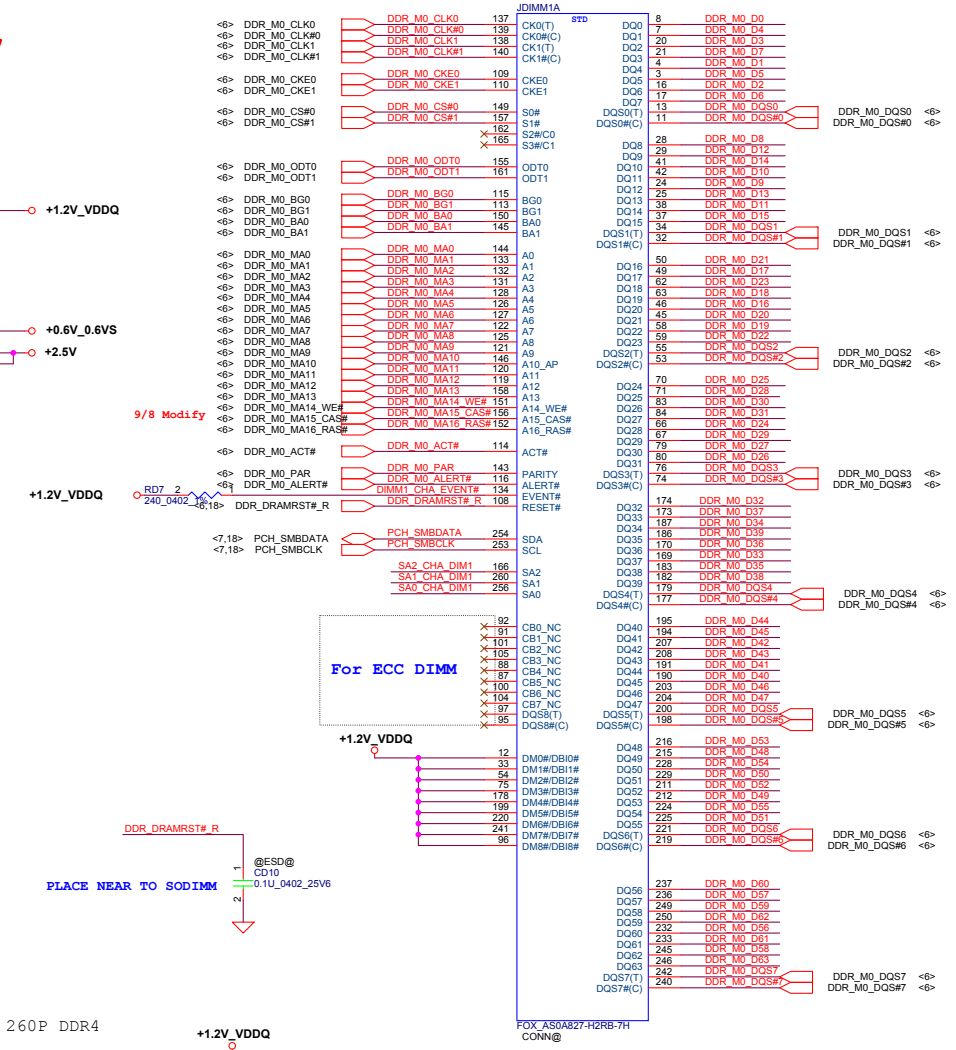
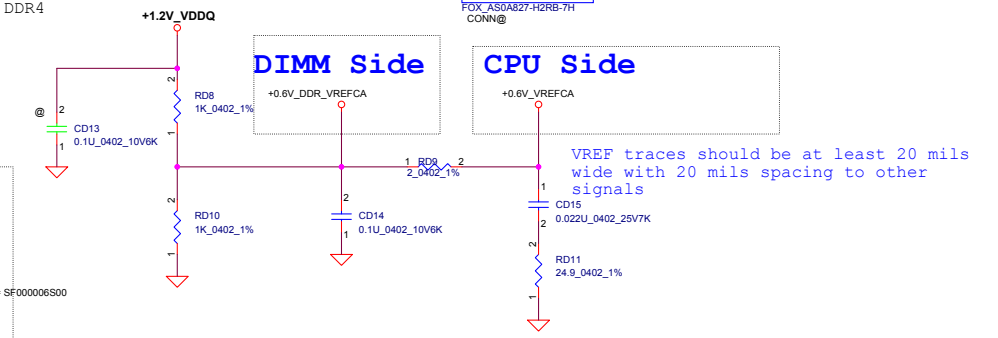




Part Number:LTCX0069GA0
Part Value:S SOCKET FOX AS0A827-H2RB-7H 260P DDR4





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Issued Date	2017/04/10	Deciphered Date 2019/12/15	Title: P18-DDRIV_CHA: DIMM0
			Size: B; Document Number: LA-G07DP(KBL-U_UMA_6L); Rev: v0.3
			Date: Friday, January 05, 2018; Sheet 17 of 59

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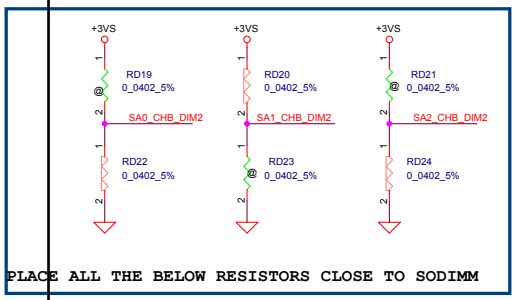
CHANNEL-B

STD (5.2 mm)

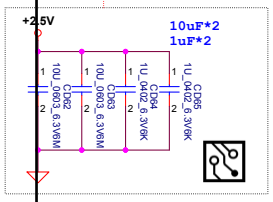
TOP: JDIMM2 CONN Non-ECC DIMM



PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM2.257,259



Layout Note:
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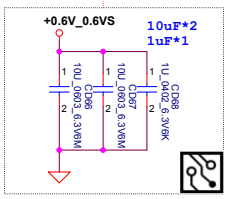
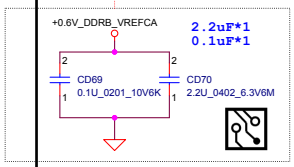
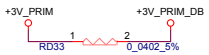
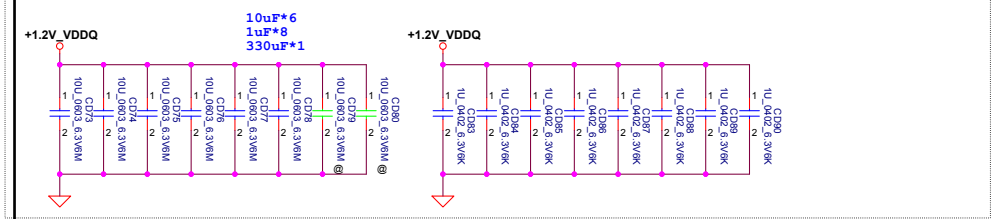


Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2

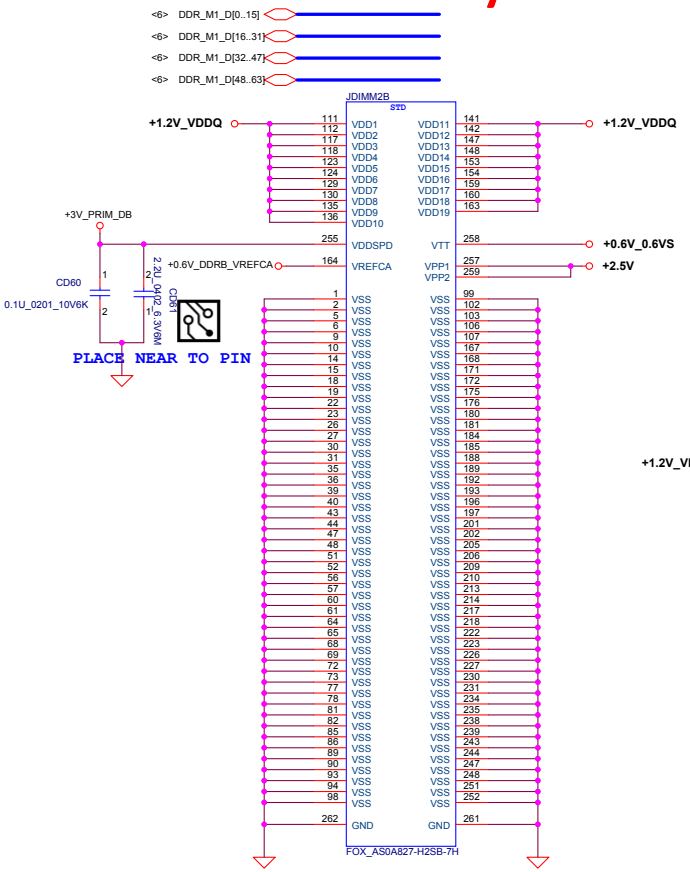




Layout Note:
Place near JDIMM2



Interleaved Memory



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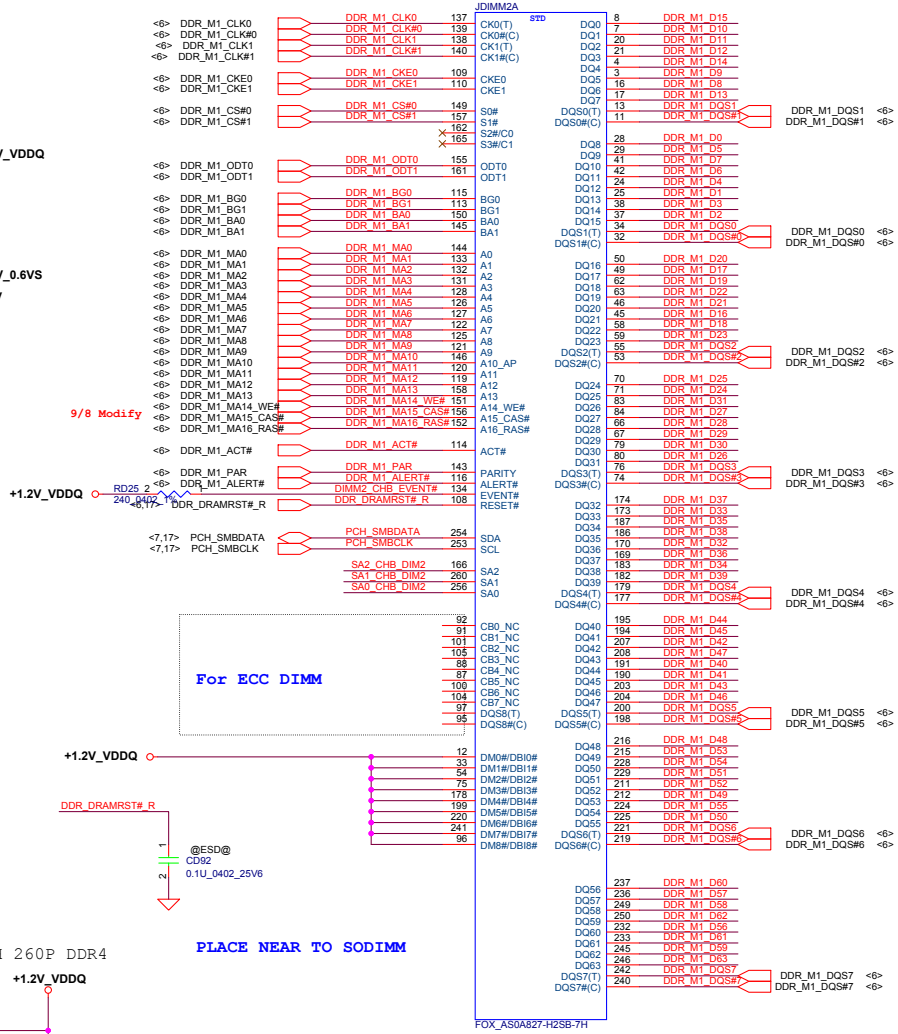
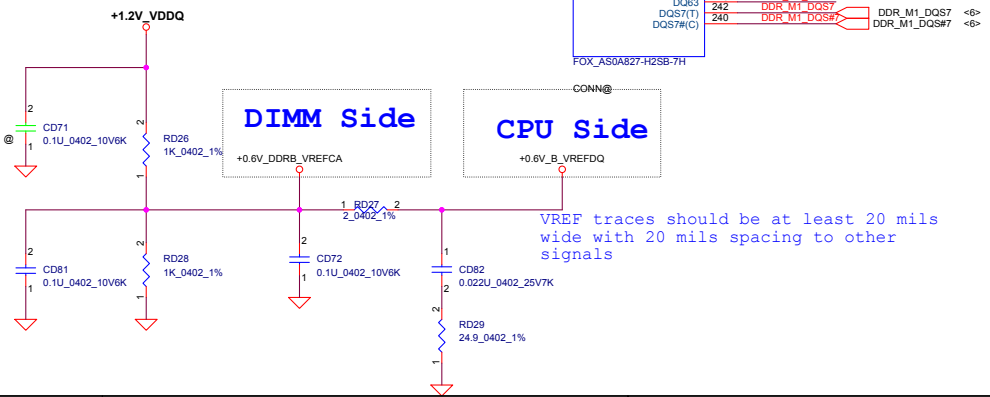
Part Value:S SOCKET FOX AS0A827-H2SB-7H 260P DDR4



PLACE NEAR TO SODIMM



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			Size: B — Document Number: LA-G07DP(KBL-U UMA 6L) — Rev: v0.3
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Title	NV(4/5)-GPIO/Strap	
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Title	NV(5/5)-MEMORY FBA		
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Title: **DGPU_DC/DC Interface**

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Title: *N16P GDDR5 A Upper Half*

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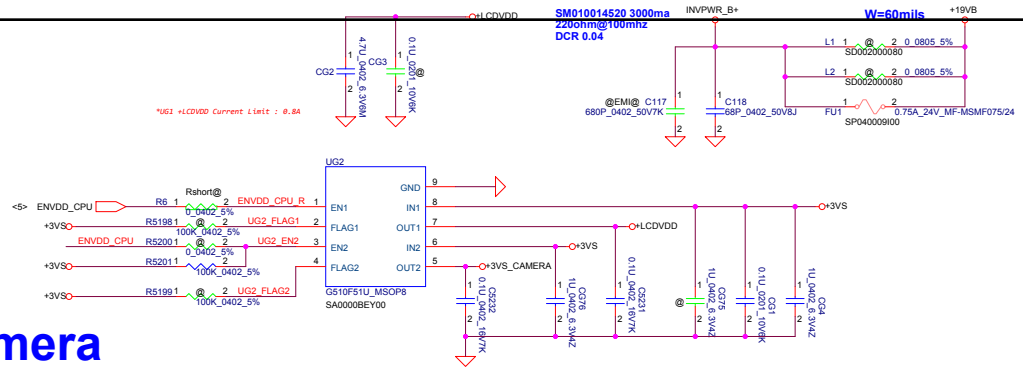
eDP Power



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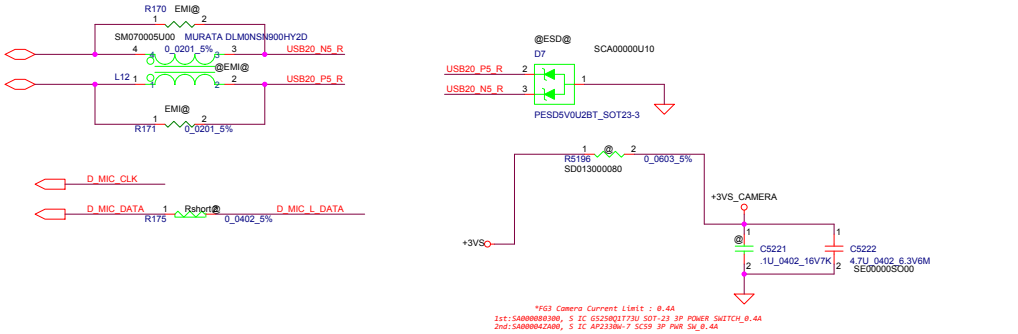

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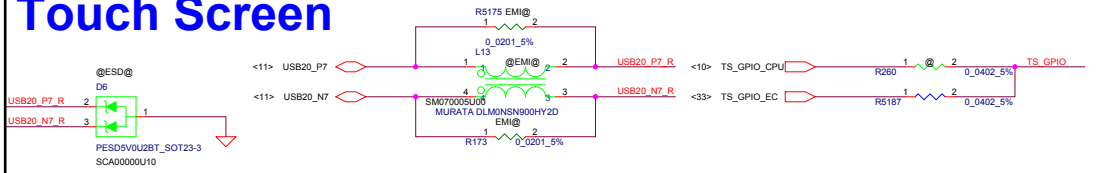

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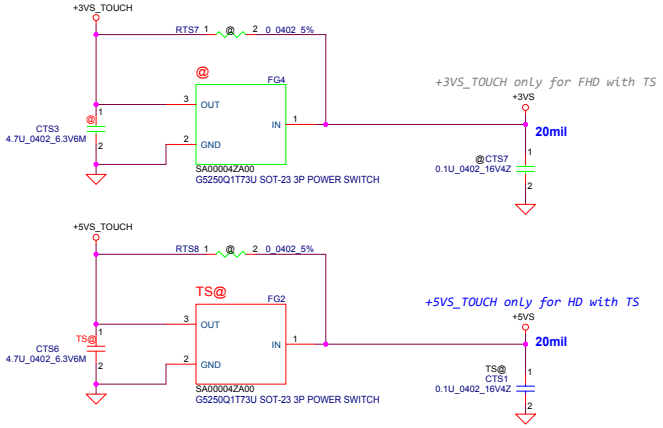

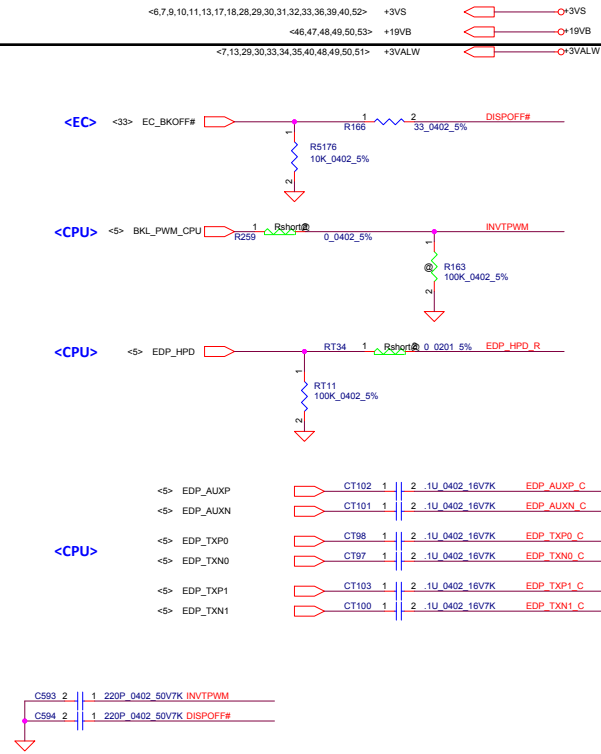

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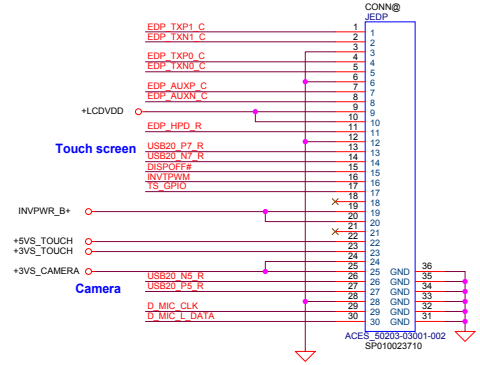

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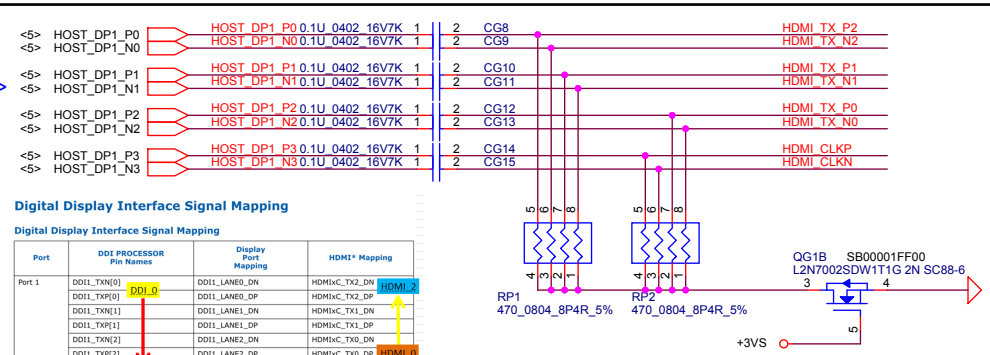
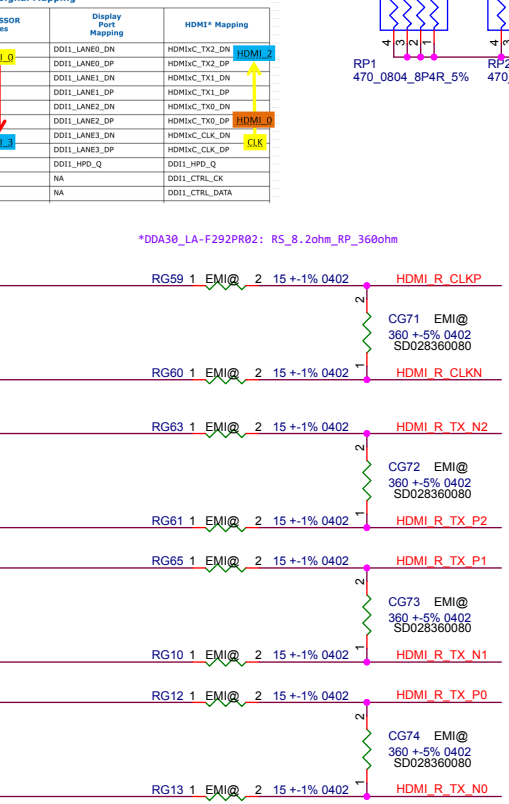


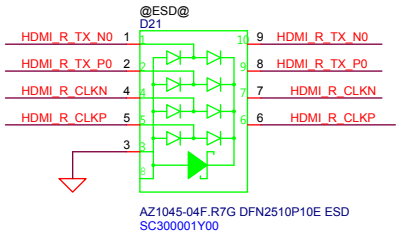
1.3.2 Digital Display Interface Signal Mapping

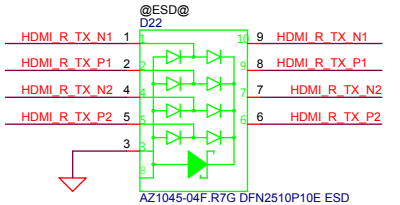
Table 1-4. Digital Display Interface Signal Mapping

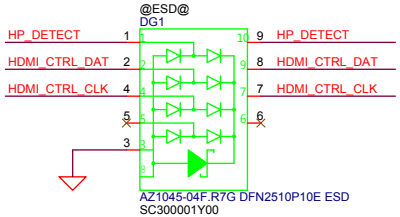
Port	DDI PROCESSOR Pin Names	Display Port Mapping	HDMI* Mapping
Port 1	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIxC_TX2_DN
	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIxC_TX2_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIxC_TX1_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIxC_TX1_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIxC_TX0_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIxC_TX0_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIxC_CLK_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIxC_CLK_DP
	DDPB_HPD	DDI1_HPD_Q	DDI1_HPD_Q
	DDPB_CTRLCLK	NA	DDI1_CTRL_CK
	DDPB_CTRLDATA	NA	DDI1_CTRL_DATA

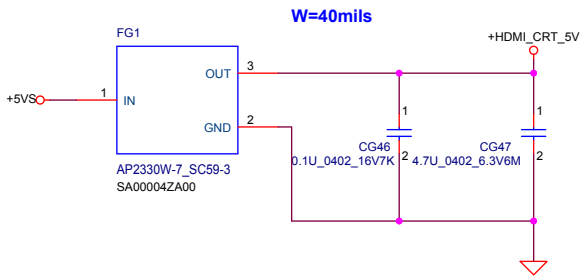
DDI_0 → HDMI_2; DDI_3 → HDMI_0 CLK

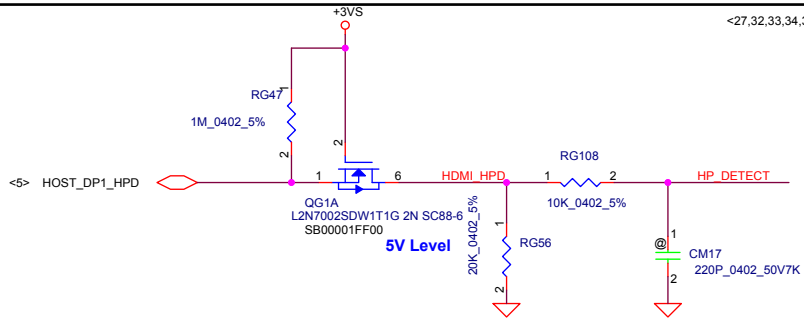


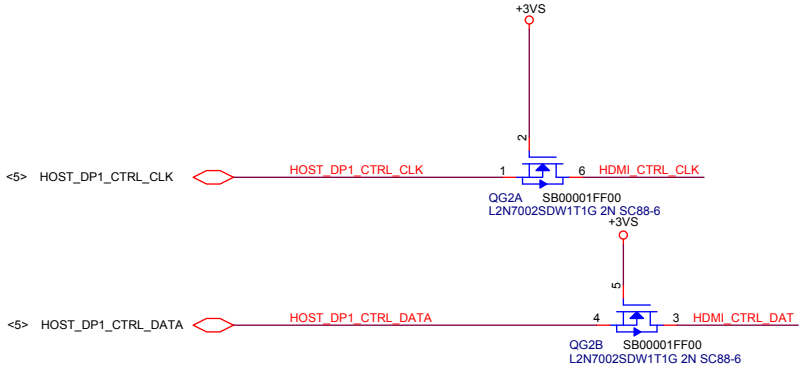


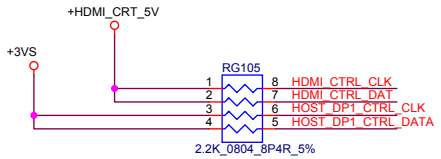




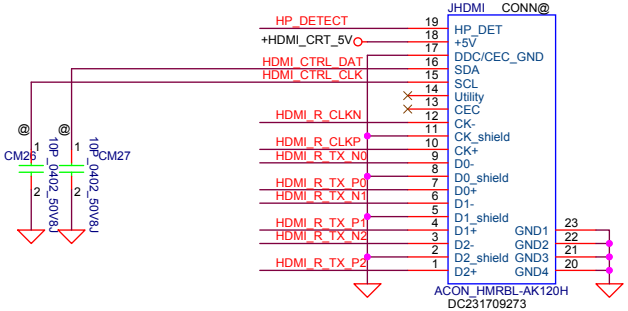








HDMI Conn.



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Title: HDMI Conn/Level shift

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+LAN_VDD_3V3 Rising time need>0.5mS and <100mS

CL8, CL23 close LL2.
CL26 close UL1 Pin 3.
CL12 close UL1 Pin 8.
CL13 ~ CL15 close UL1 Pin 22.
CL11, CL27 close UL1 Pin 30.

RTL8107ESH-CG/RTL8111HSH-CG Co-Lay

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

CL9, CL20 close to UL1 Pin 11
CL5 & CL19 close to UL1: Pin 32

CL10& CL16 close to UL1: Pin 23

(SA000084T00) RTL8111HSH-CG Giga

powe rail need to check

powe rail need to check

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<7,13,29,33,34,35,40,48,49,50,51> +3VALW

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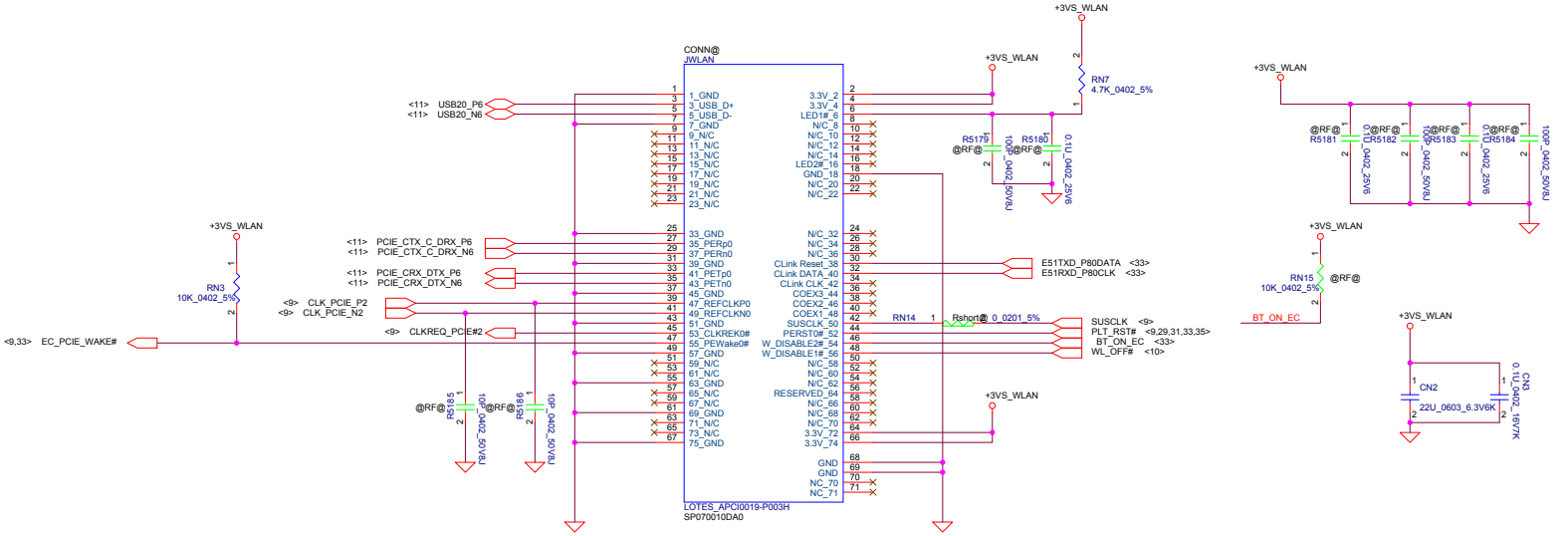
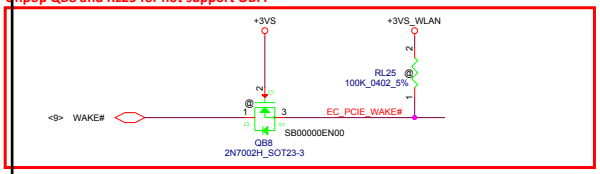


NGFF and WLAN

Unpop QB8 and RL25 for not support OBFF



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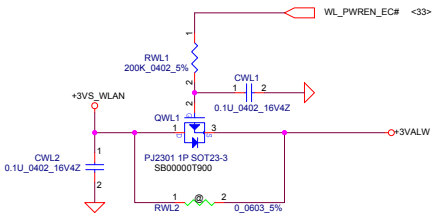

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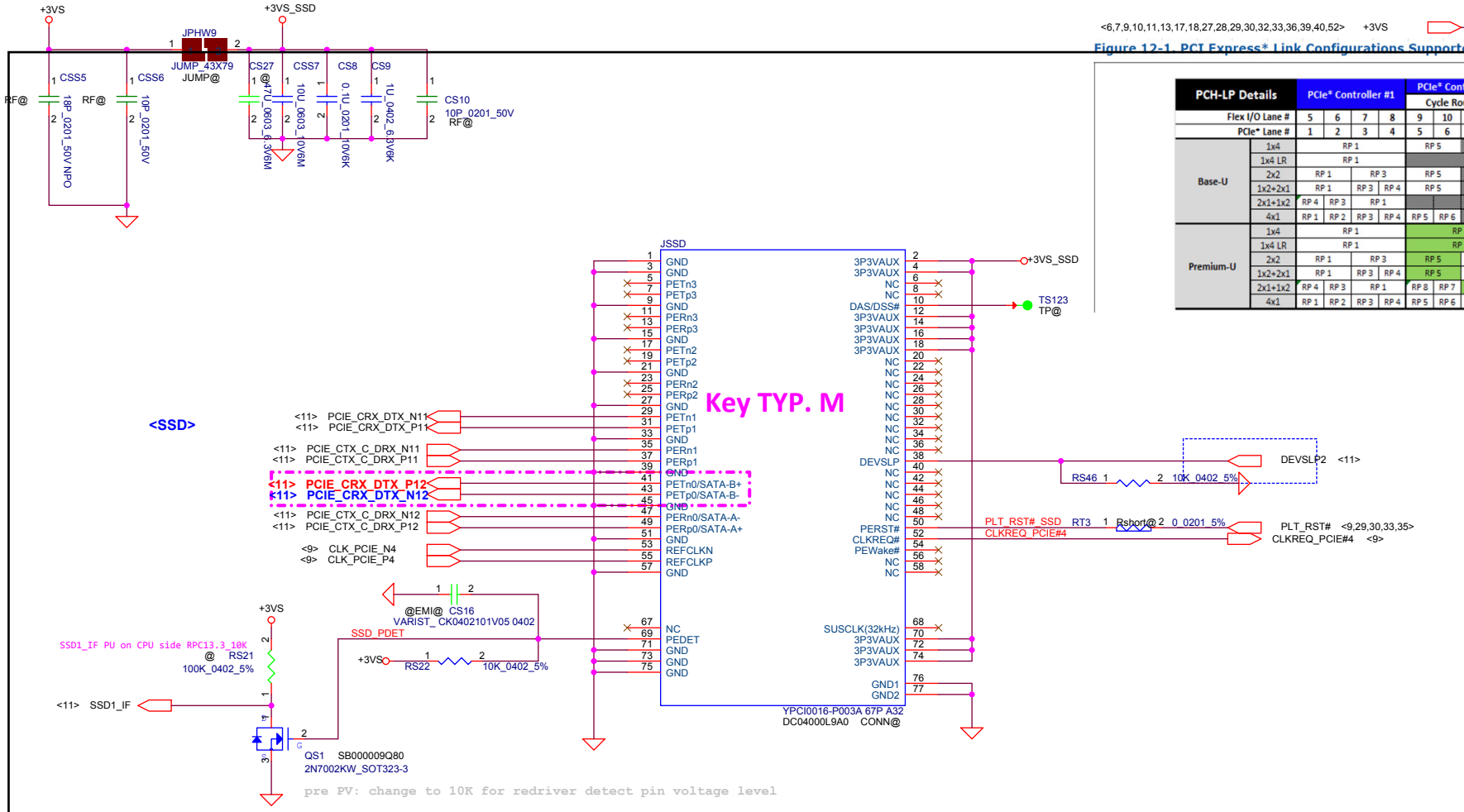

<6,7,9,10,11,13,17,18,27,28,29,30,32,33,36,39,40,52> +3VS +3VS

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2 Cycle Router #2				PCIe* Controller #3 Cycle Router #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1				RP 5				RP 9			
	1x4 LR	RP 1								RP 9			
	2x2	RP 1		RP 3		RP 5				RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1						RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6			RP 9	RP 10	RP 11	RP 12
Premium-U	1x4	RP 1				RP 5				RP 9			
	1x4 LR	RP 1				RP 5				RP 9			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12

39	GND	PCIeMVMe_DD90000NU90_MZVLW1T0HMLH-000H1 F73H1Q 0FH			39	GND	Return Current Path	40	
41	PETn0	PCIe TX	42	N/C	41	PETn0	Transmitter Differential Signal Pair	42	
43	PETp0	PCIe TX	44	N/C	43	PETp0	Transmitter Differential Signal Pair	44	
45	GND	Return current path	46	N/C	45	GND	Return Current Path	46	
47	PERn0	PCIe Rx	48	N/C	47	PERn0	Receiver Differential Signal Pair	48	
49	PERp0	PCIe Rx	50	PERST#	49	PERp0	Receiver Differential Signal Pair	50	
51	GND	Return current path	52	CLKREQ#	51	GND	Return Current Path	52	

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

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Title: *M.2 SSD*

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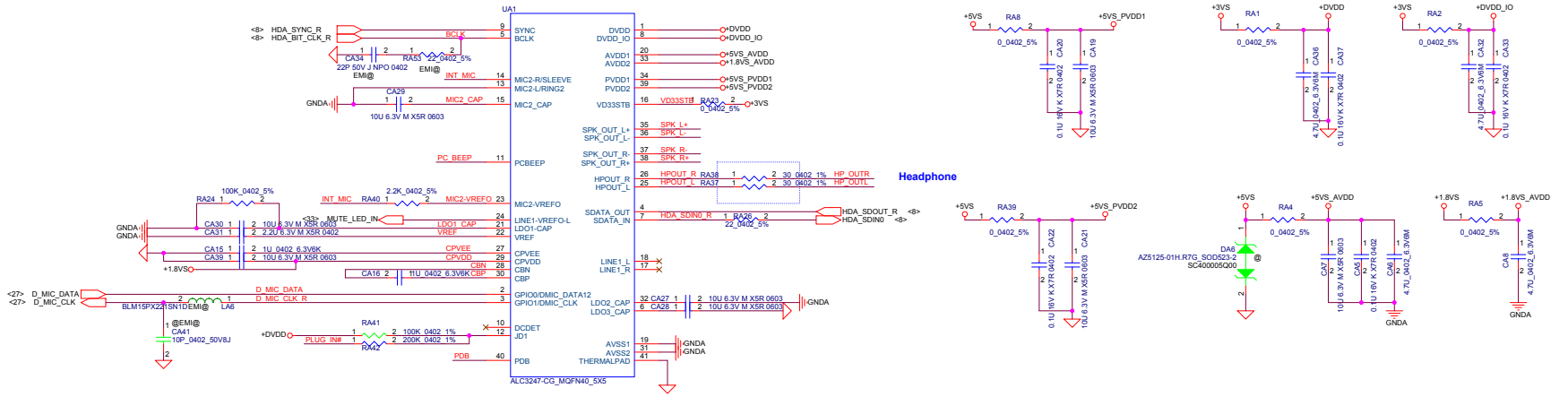
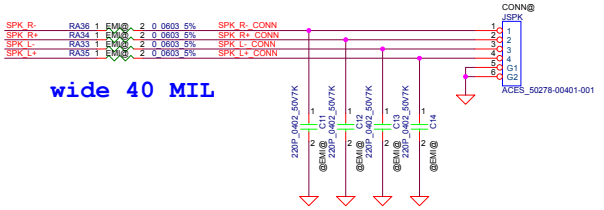
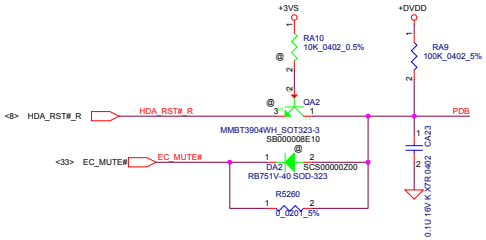
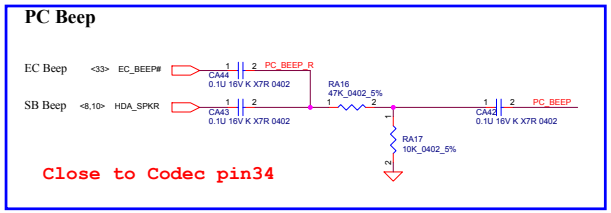


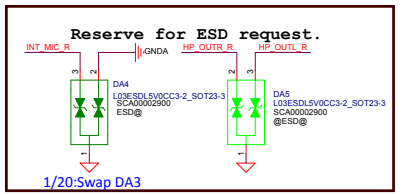
Internal SPK

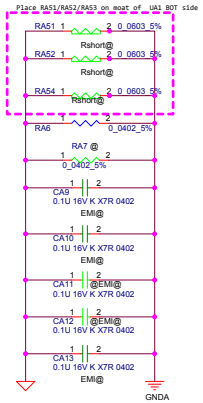


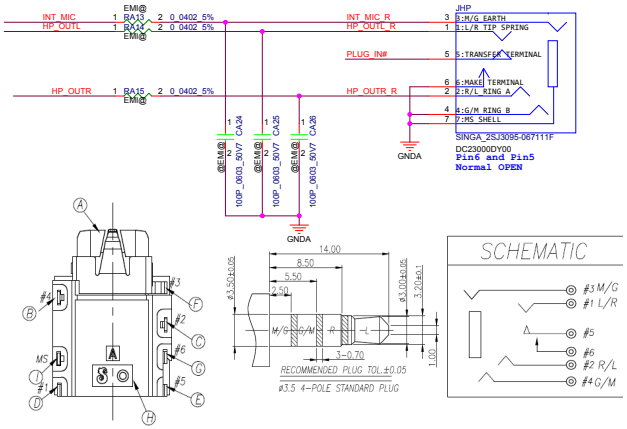


PC Beep









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EC Board ID (UMA, DIS, phase) control table

RK4	KBL-U				KBL-R			
	DB	SI	PV	MV	DB	SI	PV	MV
UMA	15K (0x04)	27K (0x06)	43K (0x08)	75K (0x0A)	130K (0x0C)	200K (0x0E)	270K (0x10)	430K (0x12)
DIS	20K (0x05)	33K (0x07)	56K (0x09)	100K (0x0B)	160K (0x0D)	240K (0x0F)	330K (0x11)	560K (0x13)

Reserve EC_CLR_CMOS for clear CMOS

(2016-03-04 : Confirm Intel platform not support EC Clear CMOS function)
(2017-10-05 : 2018OPP Add EC Clear CMOS function)

U_DB_UMA_15kohm:SD034150280, S RES 1/16W 15K +-1% 0402
U_DB_ DIS_20kohm:SD034200280, S RES 1/16W 20K +-1% 0402
U_SI_UMA_27kohm:SD034270280, S RES 1/16W 27K +-1% 0402
U_SI_ DIS_33kohm:SD034330280, S RES 1/16W 33K +-1% 0402
U_PV_UMA_43kohm:SD034430280, S RES 1/16W 43K +-1% 0402
U_PV_ DIS_56kohm:SD034560280, S RES 1/16W 56K +-1% 0402
U_MV_UMA_75kohm:SD034750280, S RES 1/16W 75K +-1% 0402
U_MV_ DIS_100kohm:SD034100380, S RES 1/16W 100K +-1% 0402
R_DB_UMA_130kohm:SD034130380, S RES 1/16W 130K +-1% 0402
R_DB_ DIS_160kohm:SD034160380, S RES 1/16W 160K +-1% 0402
R_SI_UMA_200kohm:SD034200380, S RES 1/16W 200K +-1% 0402
R_SI_ DIS_240kohm:SD000001880, S RES 1/16W 240K +-1% 0402
R_PV_UMA_270kohm:SD00000G280, S RES 1/16W 270K +-1% 0402
R_PV_ DIS_330kohm:SD034330380, S RES 1/16W 330K +-1% 0402

RK106 2_0_0402_5% → CLR_CMOS# <9>
EC_CLR_CMOS → Q51 2N7002K_SOT23-3 SB00000EN00
R483 10K_0402_5%

Pin Assignment

UK1 KB9022QD_LQFP128_14X14 SA000075S30

1	GATEA20/GPIO00	KBRST#/GPIO01	2
3	SERIRQ	LPC_FRAME#	4
	LPC_AD3	LPC_AD2	
	LPC_AD1	LPC_AD0	
5	LPC_AD3	LPC_AD2	7
8	LPC_AD1	LPC_AD0	10
12	CLK_PCI_EC	PCIRST#/GPIO05	13
37	EC_RST#	EC_SCI#/GPIO0E	20
38	CLKRUN#/GPIO1D		
55	KSI0/GPIO30	KSI1/GPIO31	56
57	KSI2/GPIO32	KSI3/GPIO33	58
59	KSI4/GPIO34	KSI5/GPIO35	60
61	KSI6/GPIO36	KSI7/GPIO37	62
39	KSO0/GPIO20	KSO1/GPIO21	40
41	KSO2/GPIO22	KSO3/GPIO23	42
43	KSO4/GPIO24	KSO5/GPIO25	44
45	KSO6/GPIO26	KSO7/GPIO27	46
47	KSO8/GPIO28	KSO9/GPIO29	48
49	KSO10/GPIO2A	KSO11/GPIO2B	50
51	KSO12/GPIO2C	KSO13/GPIO2D	52
53	KSO14/GPIO2E	KSO15/GPIO2F	54
81	KSO16/GPIO48	KSO17/GPIO49	82
77	EC_SMB_CLK1/GPIO44	EC_SMB_DAT1/GPIO45	78
79	EC_SMB_CLK2/GPIO46	EC_SMB_DAT2/GPIO47	80
6	PM_SLP_S3#/GPIO04	GPIO07	14
15	GPIO08	GPIO0A	16
17	GPIO0B	GPIO0C	18
19	AC_PRESENT/GPIO0D	PWM2/GPIO11	25
28	FAN_SPEED1/GPIO14	FANFB1/GPIO15	30
31	EC_TX/GPIO16	EC_RX/GPIO17	32
34	PCH_PWROK/GPIO18	SUSP_LED#/GPIO19	36
122	NUM_LED#/GPIO1A	PBTN_OUT#/GPIO5D	123
	PM_SLP_S4#/GPIO5E		
21	EC_VCCST_PG/GPIO0F	BEEP#/GPIO10	23
26	EC_FAN_PWM/GPIO12	AC_OFF/GPIO13	27
63	VCIN1_BATT_TEMP/AD0/GPIO38	VCIN1_BATT_DROP/AD1/GPIO39	64
65	ADP_I/AD2/GPIO3A	AD_BID/AD3/GPIO3B	66
75	AD4/GPIO42	AD5/GPIO43	76
68	DA0/GPIO3C	EN_DFAN1/DA1/GPIO3D	70
71	DA2/GPIO3E	DA3/GPIO3F	72
83	EC_MUTE#/PSCLK1/GPIO4A	USB_EN#/PSDAT1/GPIO4B	84
85	PSCLK2/GPIO4C	PSDAT2/GPIO4D	86
87	TP_CLK/GPIO4E	TP_DATA/GPIO4F	88
97	ENBKL/GPIXOA00	WOL_EN/GPIXOA01	98
99	ME_EN/GPIXOA02	VCIN0_PH1/GPIXOD00	109
119	MISO/GPIO5B	MOSI/GPIO5C	120
126	SPICLK/GPIO58	SPICS#/GPIO5A	128
73	EC_CIR_RX/AD6/GPIO40	SYS_PWROK/AD7/GPIO41	74
89	GPIO50	BATT_CHG_LED#/GPIO52	90
91	CAPS_LED#/GPIO53	PWR_LED#/GPIO54	92
93	BATT_LOW_LED#/GPIO55	SYSON/GPIO56	95
121	VR_ON/GPIO57	DPWROK_EC/GPIO59	127
100	EC_RSMRST#/GPIXOA03	GPIXOA04	101
102	VCIN1_ADP_PROCHOT/GPIXOA05	VCOUT1_PROCHOT#/GPIXOA06	103
104	VCOUT0_MAIN_PWR_ON/GPIXOA07	BKOFF#/GPIXOA08	105
106	GPIXOA09	PCH_PWR_EN/GPIXOA10	107
108	PWR_VCCST_PG/GPIXOA11		
110	VCIN1_AC_IN/GPIXOD01	ALW_PWE_EN EC_ON/GPIXOD02	112
114	ON/OFF#/GPIXOD03	LID_SW#/GPIXOD04	115
116	SUSP#/GPIXOD05	GPIXOD06	117
118	PECI/GPIXOD07		
124	V18R/VCC_IO2		

Power Rails

9	VCC_LPC	22	VCC
33	VCC	61	VCC
125	VCC	67	AVCC
11	GND	24	GND
52	GND	93	GND
113	GND	69	AGND

Pin111:VCC0

Signal Groups

- PWM Output
- LPC & MISC
- AD Input
- DA Output
- PS2 Interface
- Int. K/B Matrix
- SPI Device Interface
- SPI Flash ROM
- GPIO
- SM Bus
- GPIO GPO
- GPI

20mil

Key Components

- RK1 0_0603_5%
- CK1 0.1U_0201_10V6K
- CK2 0.1U_0201_10V6K
- CK3 0.1U_0201_10V6K
- LK1 SM01000Q500 S SUPPRE_ TAI-TECH HCB1005KF-221T15 0402
- LK2 SM01000Q500 TAI-TECH HCB1005KF-221T15 0402
- RK2 100K_0402_1%
- BOARD_ID
- U_PX@ RK4 56K +-1% 0402 SD034560280
- U_UMA@ RK4 43K +-1% 0402 SD034430280
- R_PX@ RK4 330K +-1% 0402 SD034330280
- R_UMA@ RK4 270K +-1% 0402 SD00000G280
- RK3 0_0402_5%
- CK8 4.7U_0402_6.3V6M
- ESD@ CK4 0.1U_0402_25V6 PLT_RST#
- RK7 330K_0402_5% EC_RST#
- CK5 0.1U_0402_16V7K
- CK9 22P 50V J NPO 0402 EMI@
- RK109 22_0402_5% EMI@
- CLK_PCI_LPC
- RK6 0_0402_5%
- R4958 VCIN1_ACOK_R 0_0402_5%
- R5094 VCIN1_AC_IN_R 0_0402_5%
- R4960 VCIN1_AC_IN_R 0_0402_5%
- For Solve tPCH04(Min 9ms) Sequence Timing
- RK15 2_0_0402_5% EC_SMB_CK2_R
- RK16 2_0_0402_5% EC_SMB_DA2_R
- RK28 100K_0402_5% MUTE_LED_OUT
- RK26 100K_0402_5% E51TXD_P80DATA
- RK20 100K_0402_5% PCH_PWROK
- RK108 10K_0402_5% MUTE_LED_IN
- RK21 10K_0402_5%
- DK2 SCS00000Z00 RB751V-40 SOD-323 NMI_DBG#_CPU <5,10>
- R5178 2_0_0201_5%
- RK8 2_0_0402_5% PROCHOT# <5>
- QK1 2N7002_SOT23-3 SB00000EN00 H_PROCHOT#_EC
- RK91 2_0_0402_5%
- RK12 4.7K_0402_5% TP_CLK
- RK13 4.7K_0402_5% TP_DATA
- RP12 100K_0804_8P4R_5%
- R295 1K_0402_5% PBTN_OUT#
- RK107 10K_0402_5% EC_CLR_CMOS
- RK18 47K_0402_5% LID_SW#
- RP11 2.2K_0804_8P4R_5%
- RK14 10K_0402_5% EC_SCI#
- RK23 100K_0402_5% SYSON
- RK27 100K_0402_5% SUSP#
- RC369 15_0402_5% EMI@ EC_SPI_CLK
- CC144 22P 50V J NPO 0402 @EMI@

CC128 RC369 place near EC Side

EMI request

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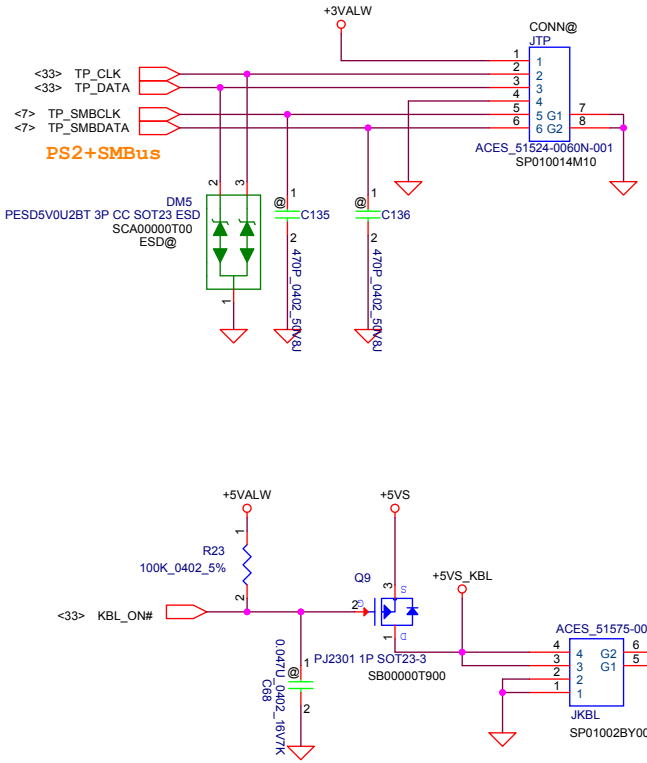
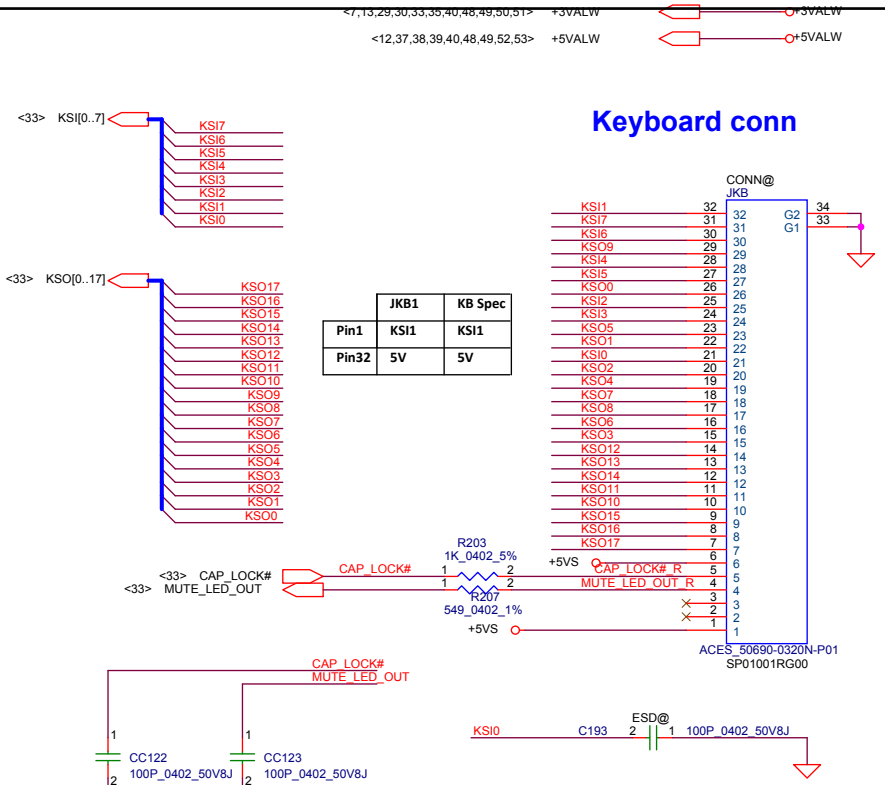
TP Button BD Connector



Keyboard conn



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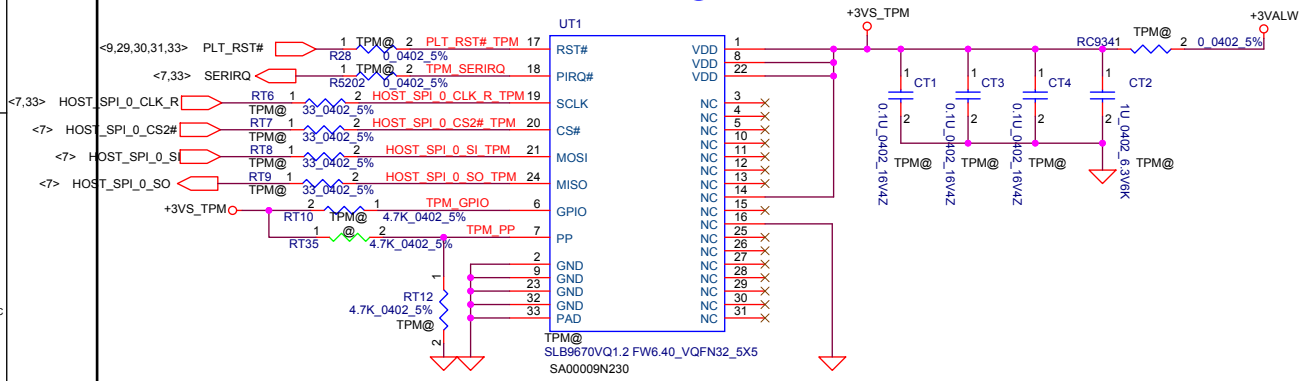
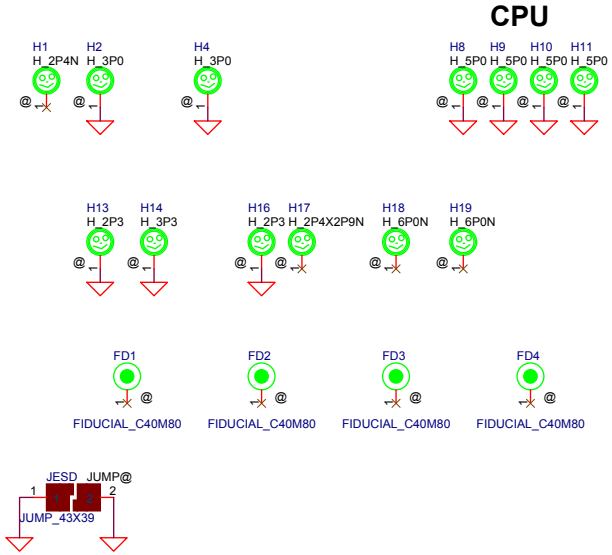
TPM2.0



Screw Hole



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Title: TPM/Screw

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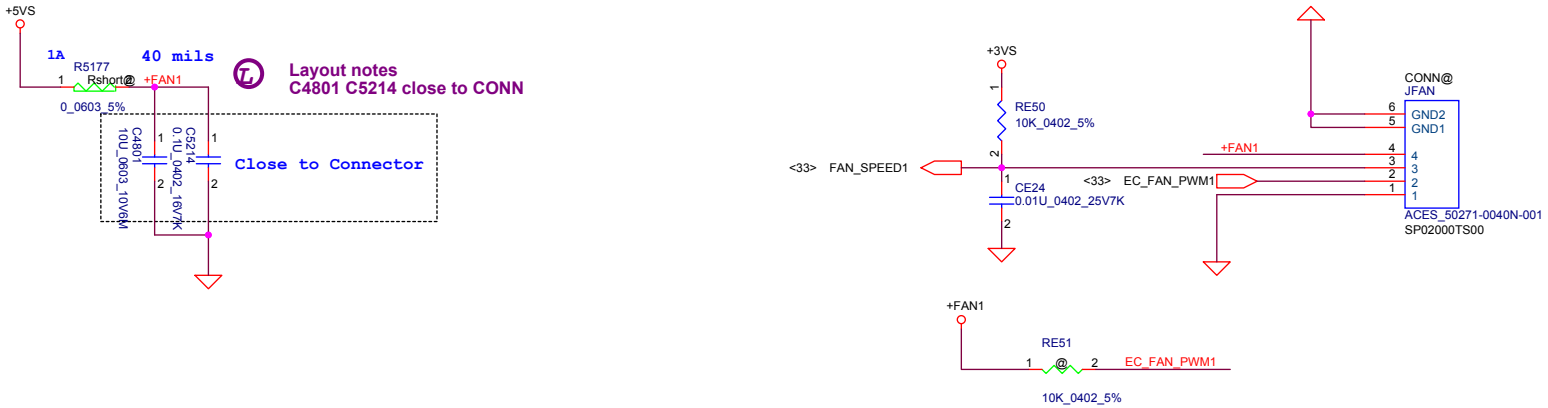

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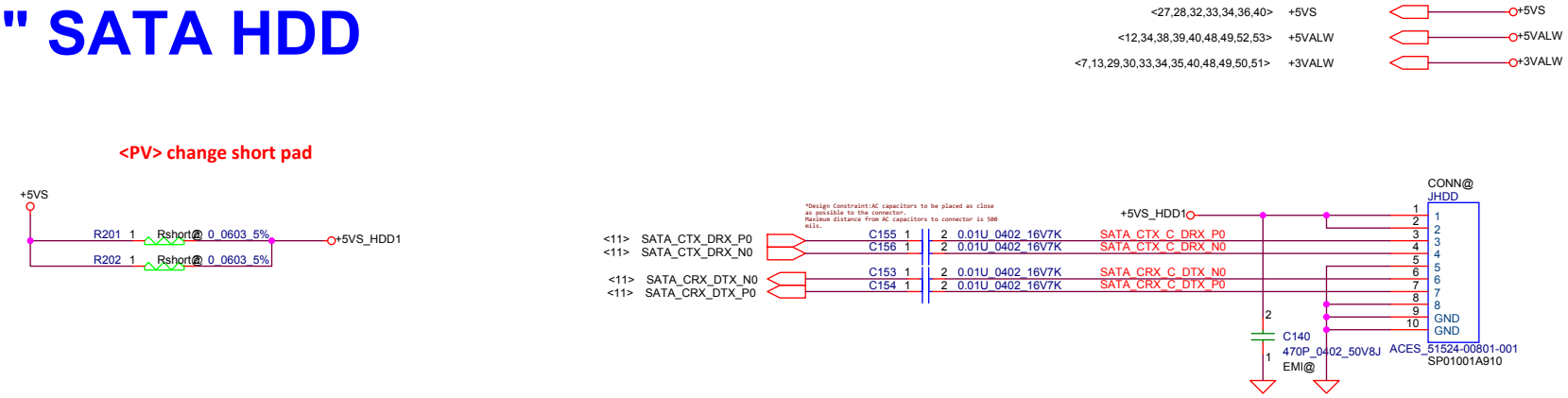
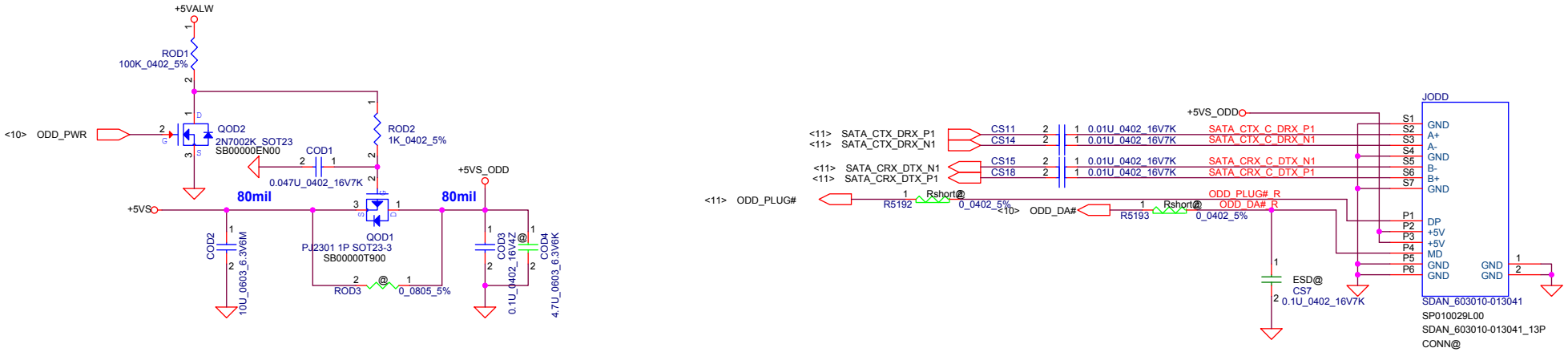
2.5" SATA HDD



SATA ODD



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Title: HDD/ODD Conn

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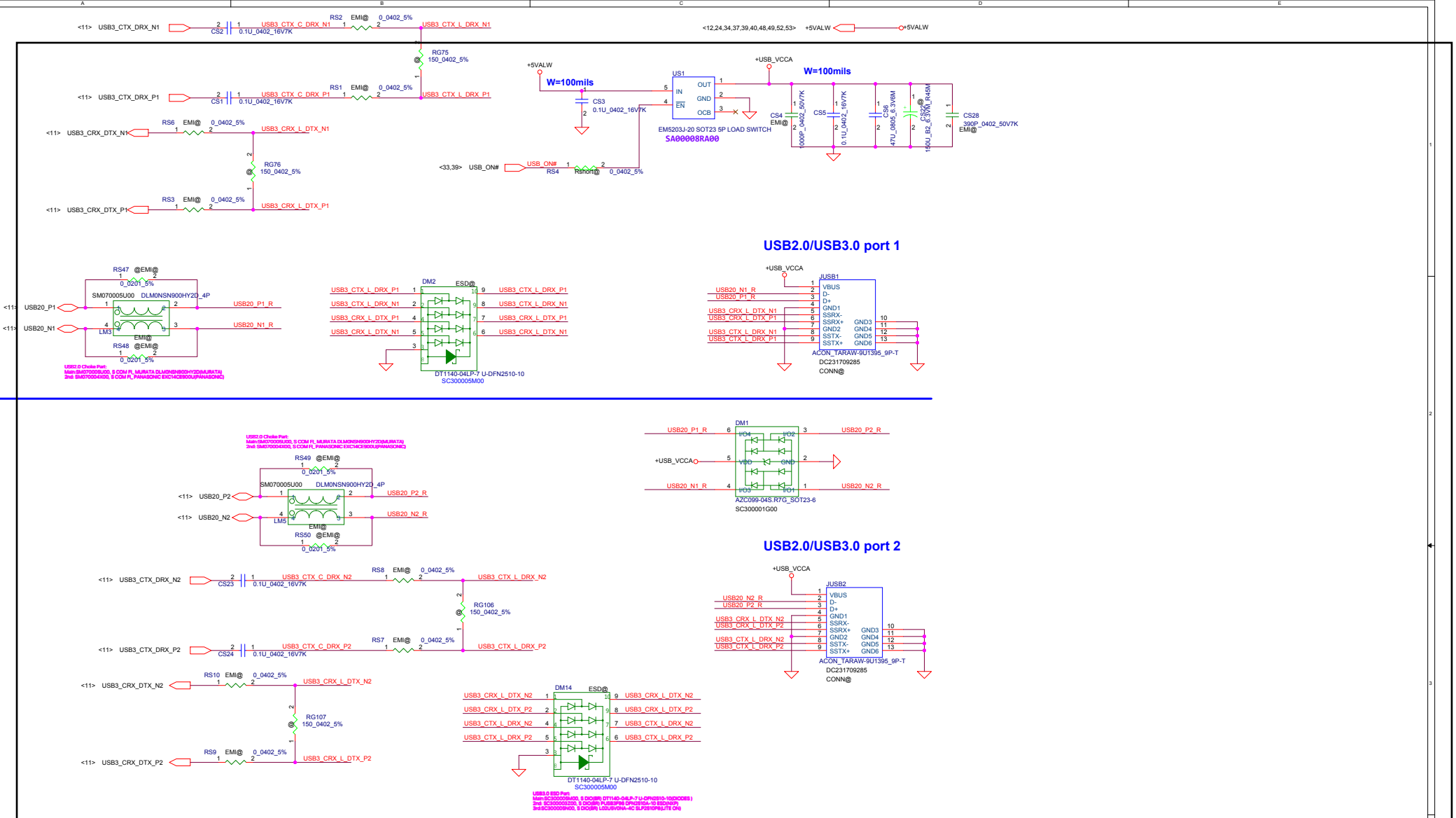

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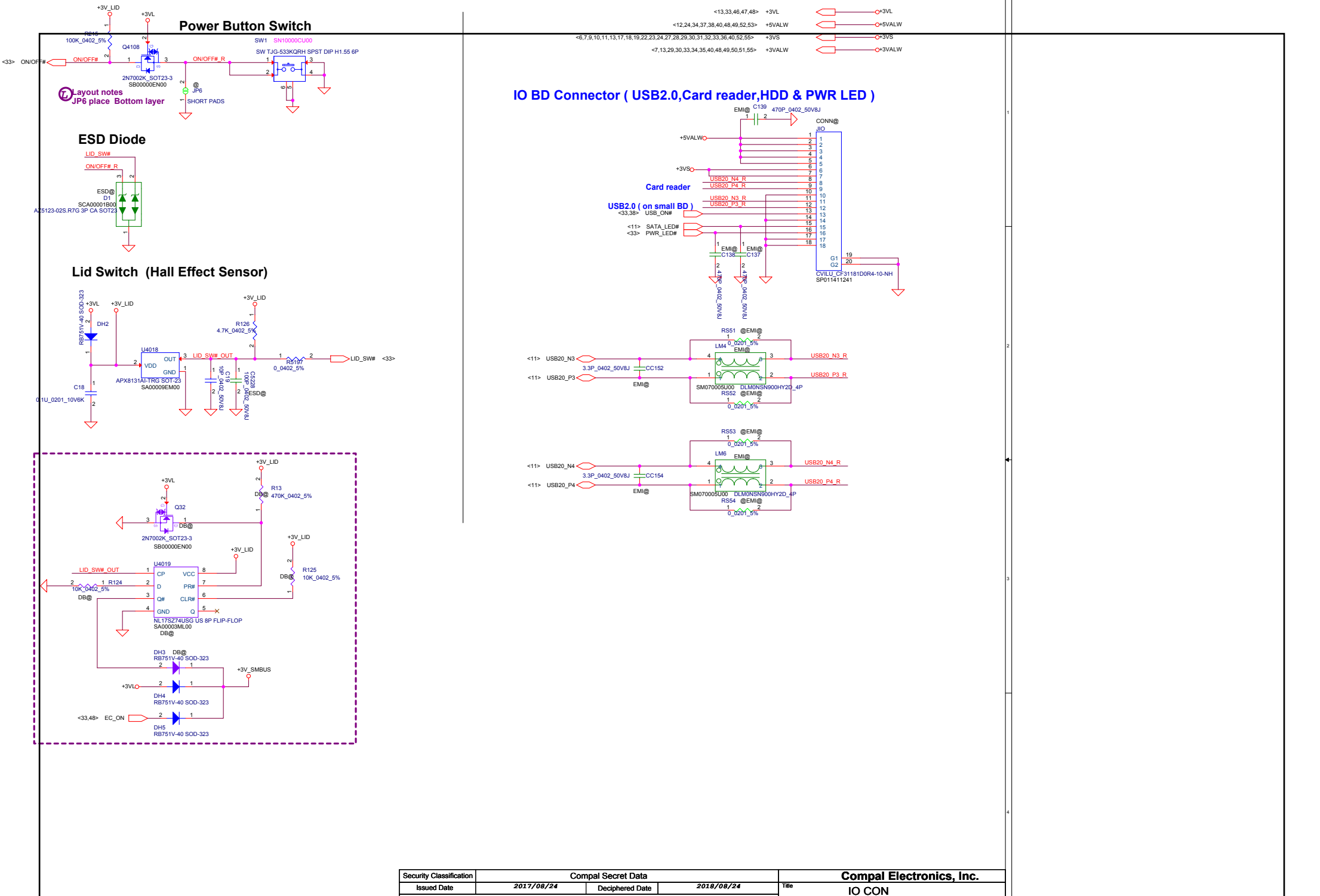

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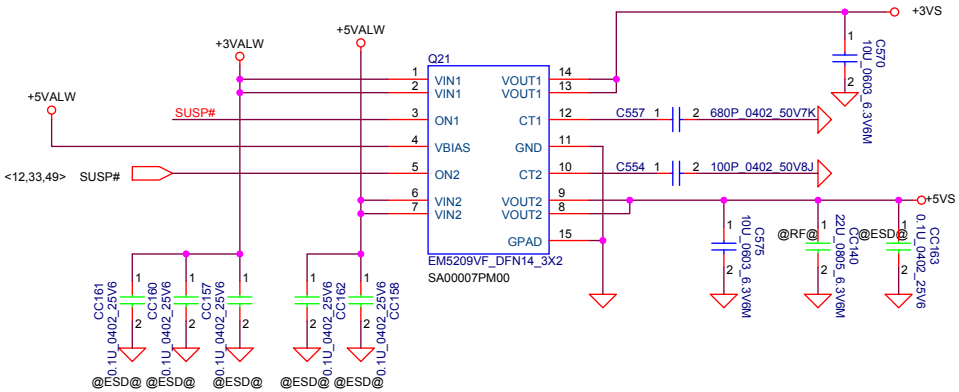
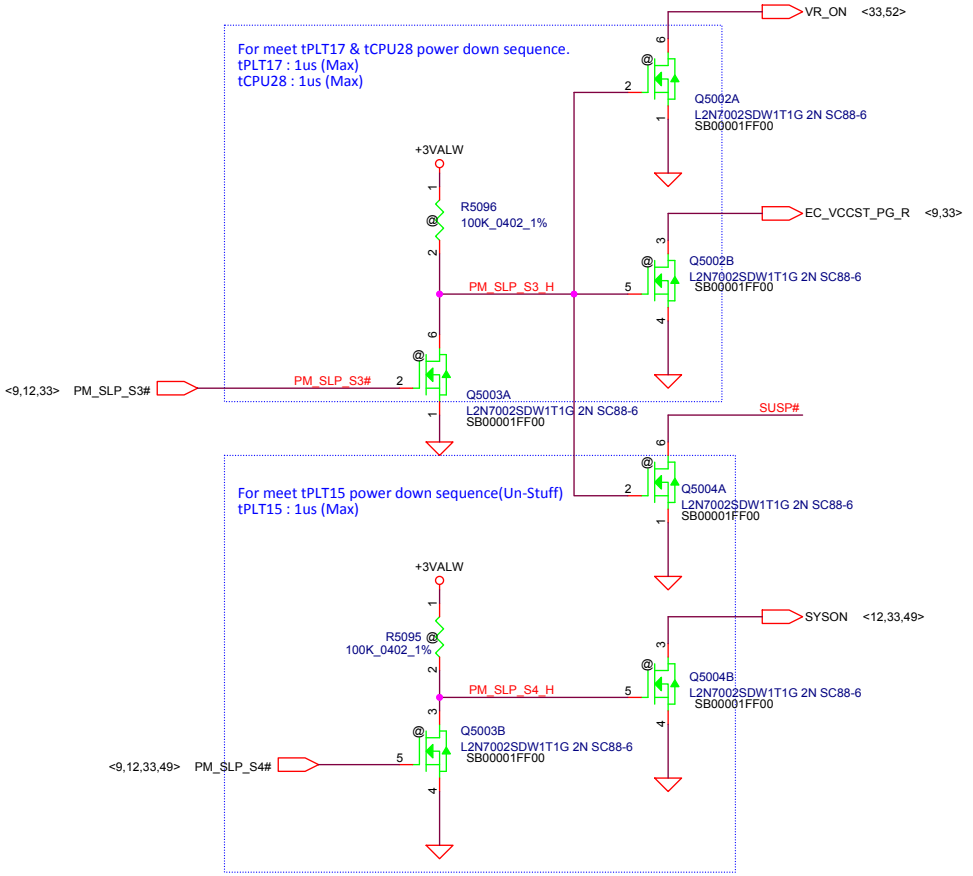
Date: Tuesday, January 09, 2018	Sheet 39 of 59		

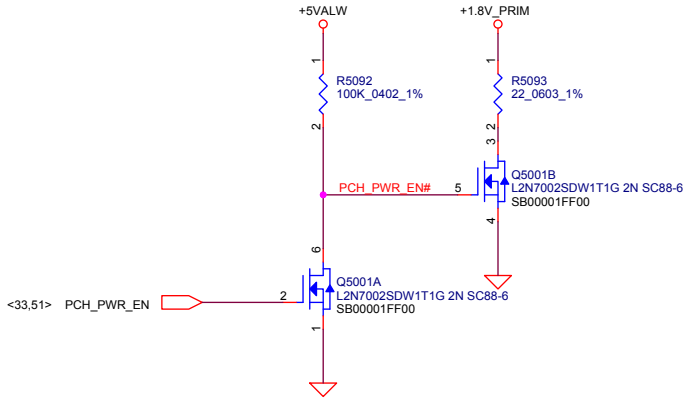
+3VS +3VS <6,7,9,10,11,13,17,18,27,28,29,30,31,32,33,36,39,52>

+5VS +5VS <27,28,32,33,34,36,37>





For +1.8V_PRIM Discharge



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

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Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA-G07DP(KBL-U_UMA_6L) | Rev: v0.3

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Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

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Compal Electronics, Inc.

Title: HW Reserve

Size	Document Number	Rev
Custom	LA-G07DP(KBL-U_UMA_6L)	v0.3

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Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

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Compal Electronics, Inc.

Title: HW Reserve

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Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

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Compal Electronics, Inc.

Title: HW Reserve

Size: Custom | Document Number: LA-G07DP(KBL-U_UMA_6L) | Rev: v0.3

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Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

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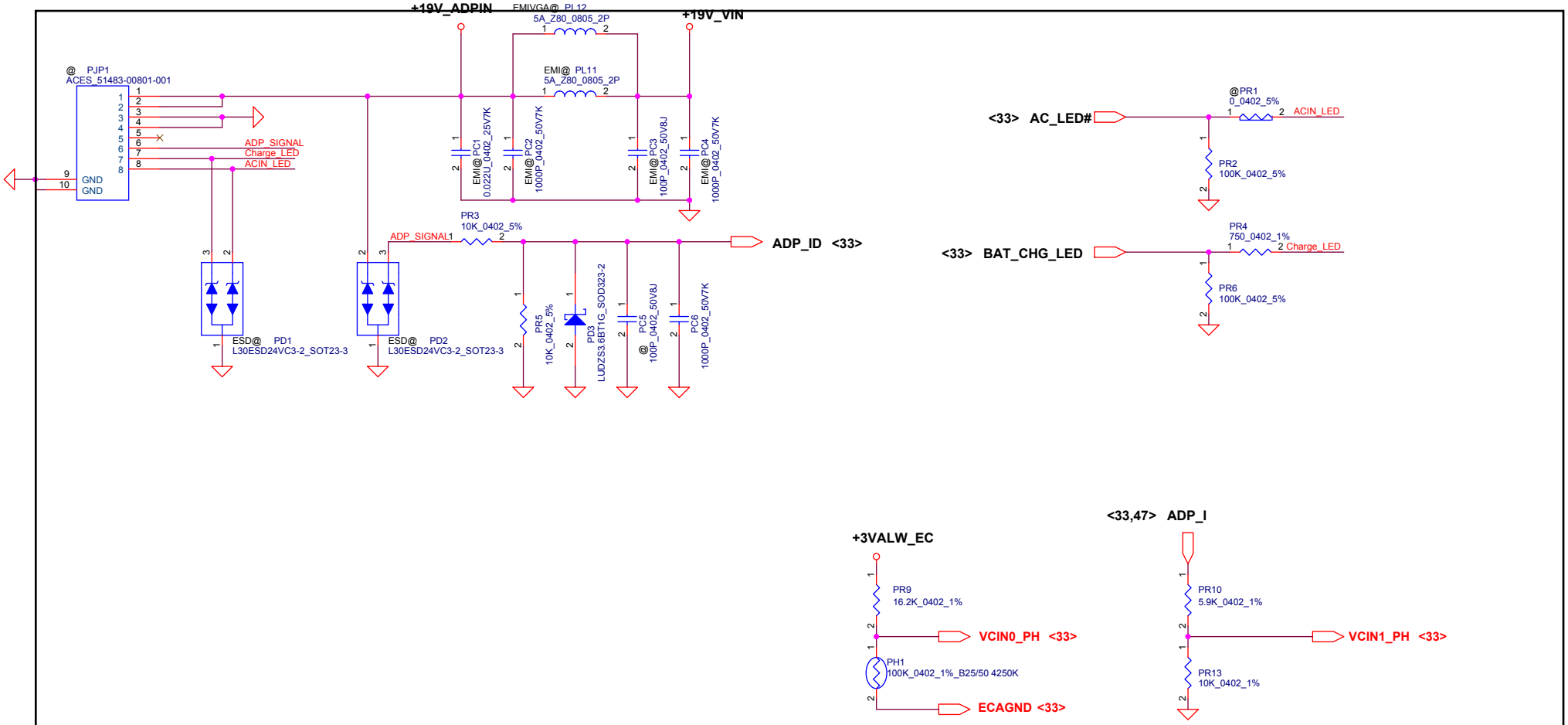
Compal Electronics, Inc.

Title: HW Reserve

Size: Custom | Document Number: LA-G07DP(KBL-U_UMA_6L) | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 44 of 59



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Issued Date	2016/09/01	Deciphered Date	2019/09/01

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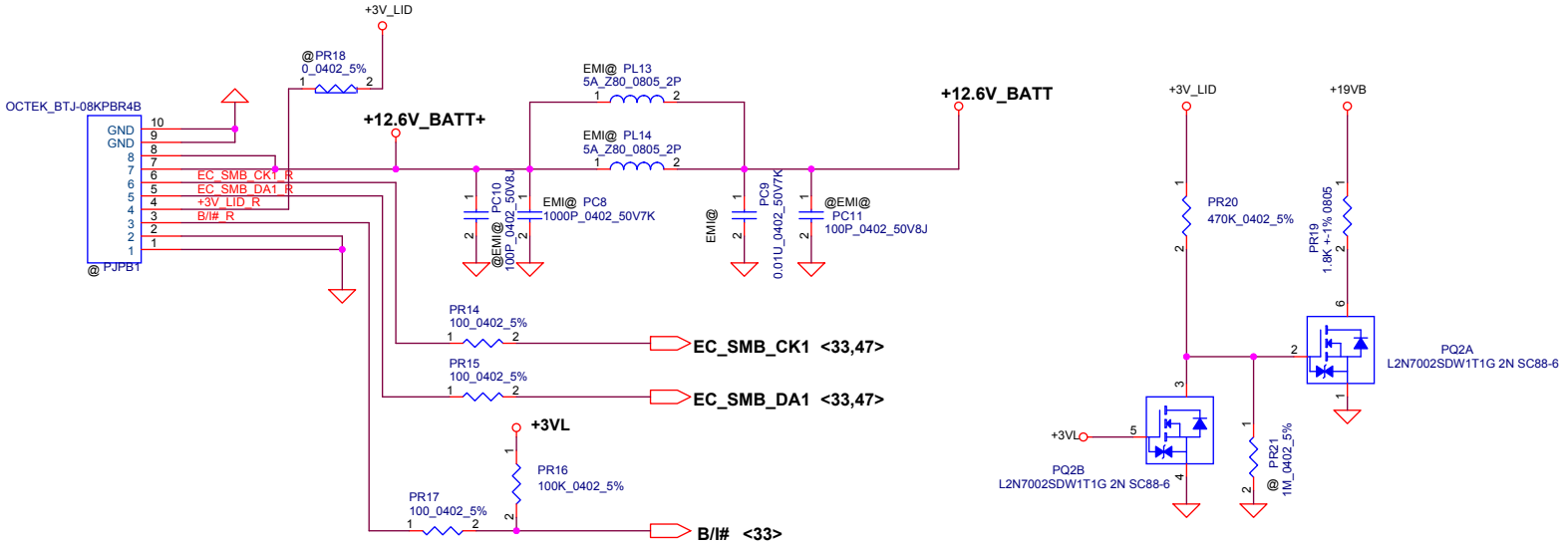
Title	DC Conn		
Size	Document Number		Rev
D	LA-G07DP(KBL-U_UMA_6L)		v0.3
Date:	Friday, January 05, 2018	Sheet	45 of 59



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01	Title: BATT Conn
				Document Number: LA-G07DP(KBL-U_UMA_6L) Rev: v0.3
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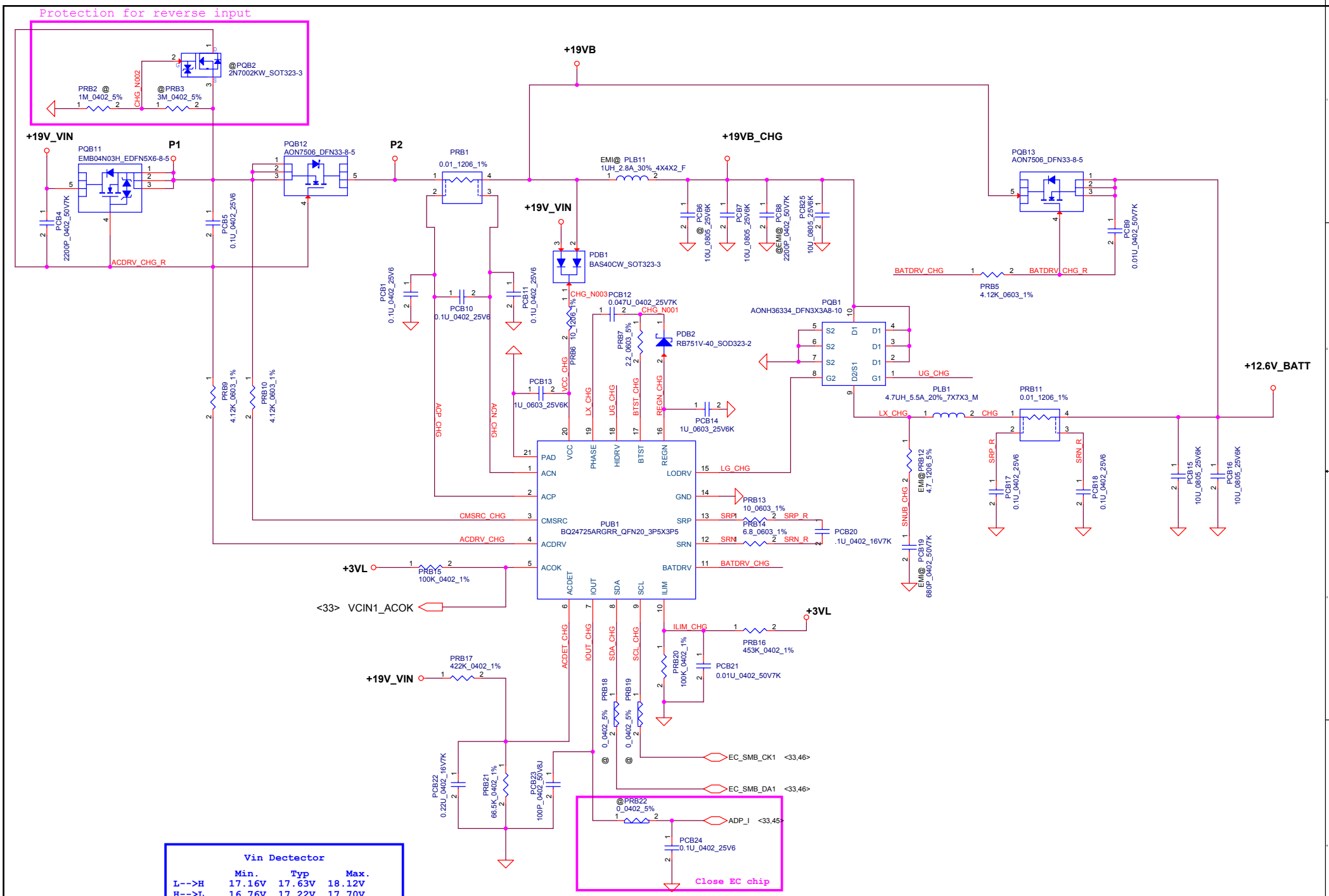

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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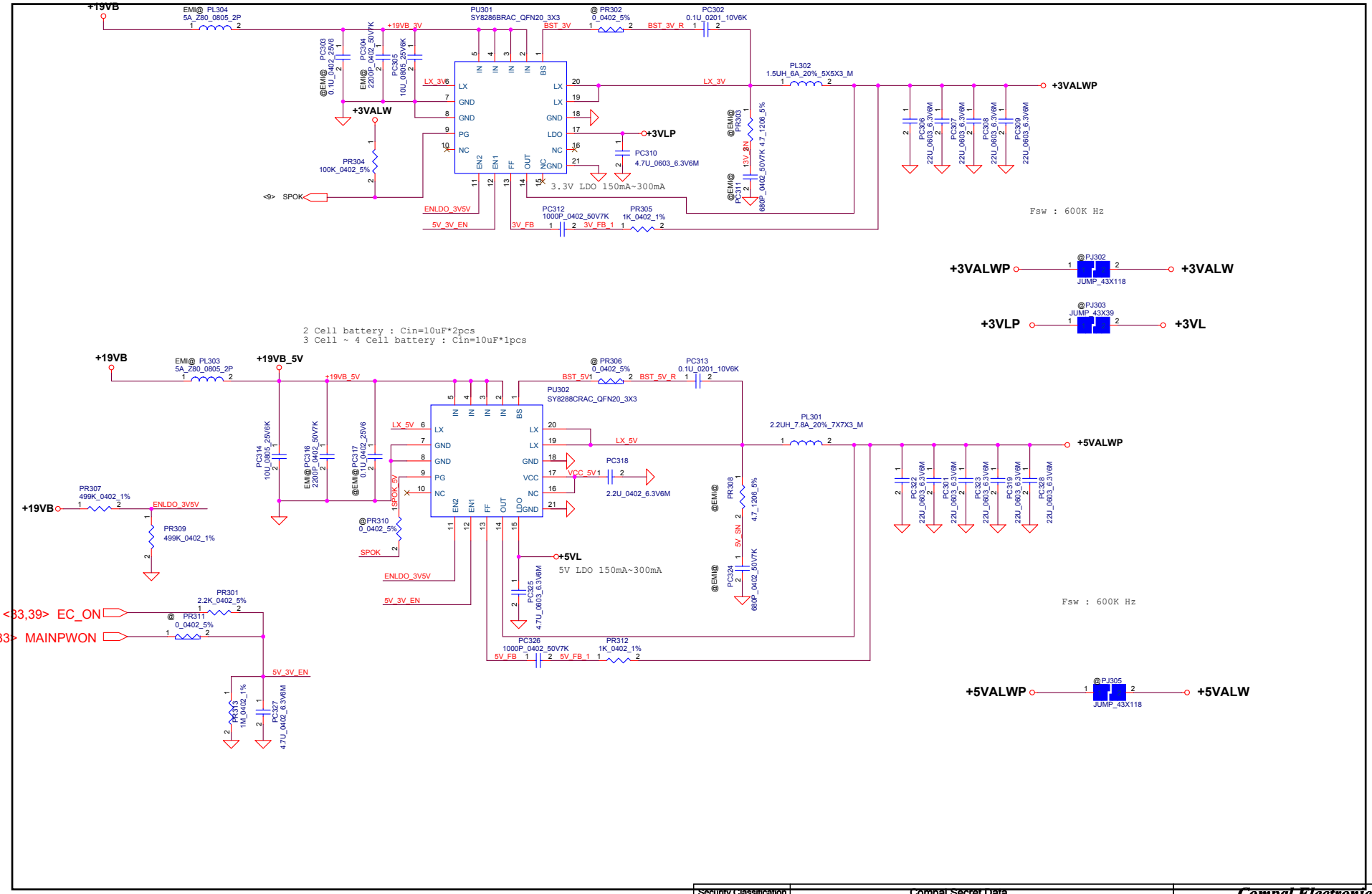
Compal Electronics, Inc.

Title: CHARGER

Document Number: | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 47 of 59



Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Compal Electronics, Inc.			
Title	3VALW/5VALW		
Size: Custom	Document Number: LA-G07DP(KBL-U_UMA_6L)		Rev: v0.3
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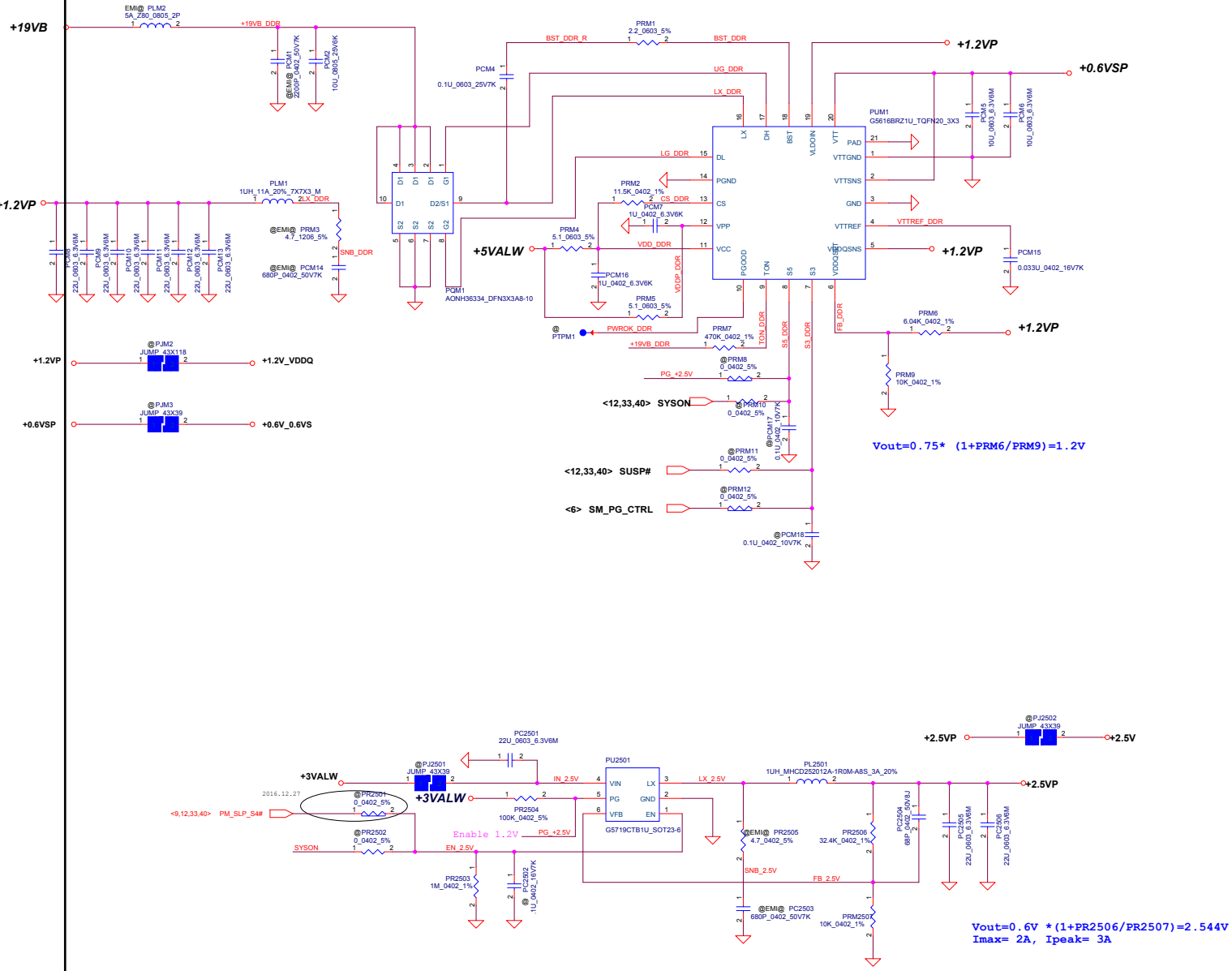

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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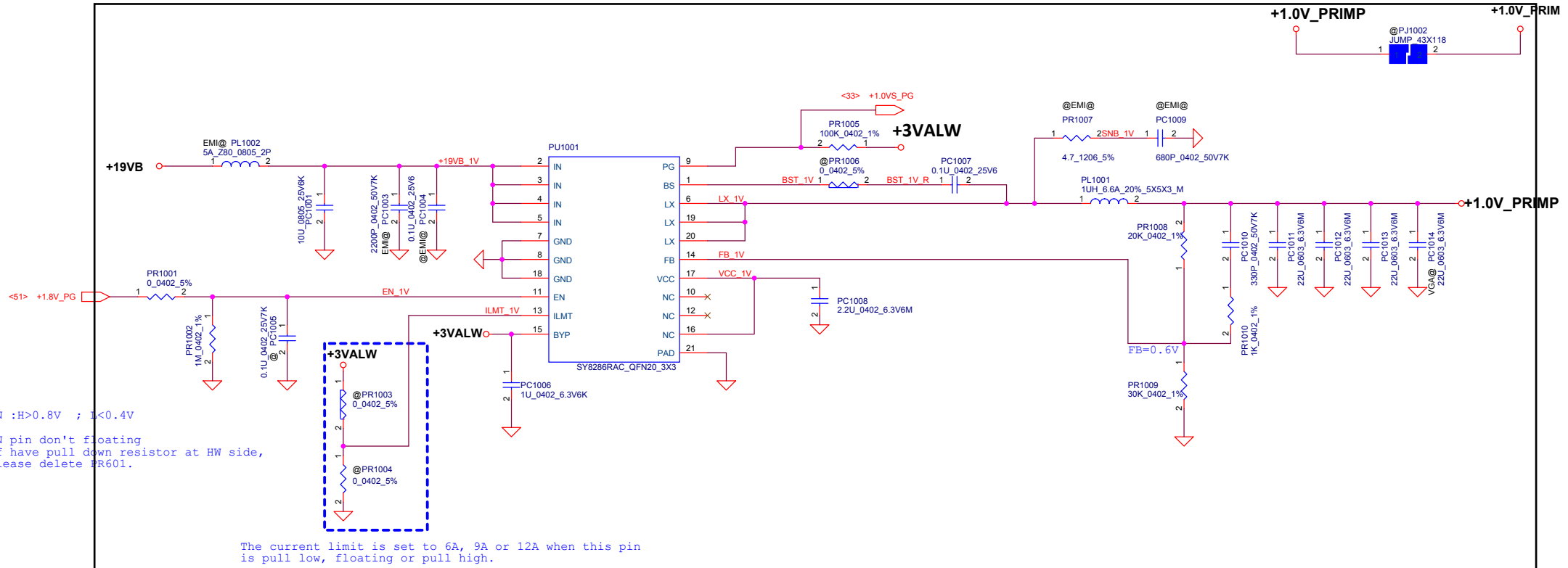
Compal Electronics, Inc.			
Title: 1.2VP/0.6VSP/2.5V			
Size: Custom	Document Number		Rev: v0.3
Date: Friday, January 05, 2018	Sheet 49 of 59		



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Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Title: 1.0V_PRIM

Size: Custom | Document Number | Rev: v0.3

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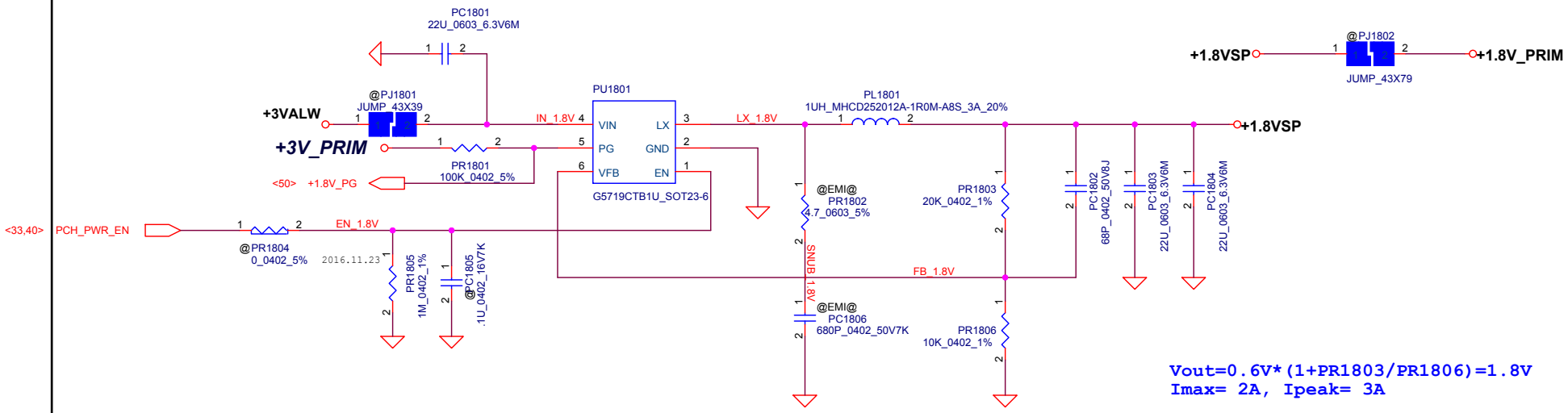

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01	Title: 1.8V_PRIM
				Size: B; Document Number: LA-G07DP(KBL-U_UMA_6L); Rev: v0.3
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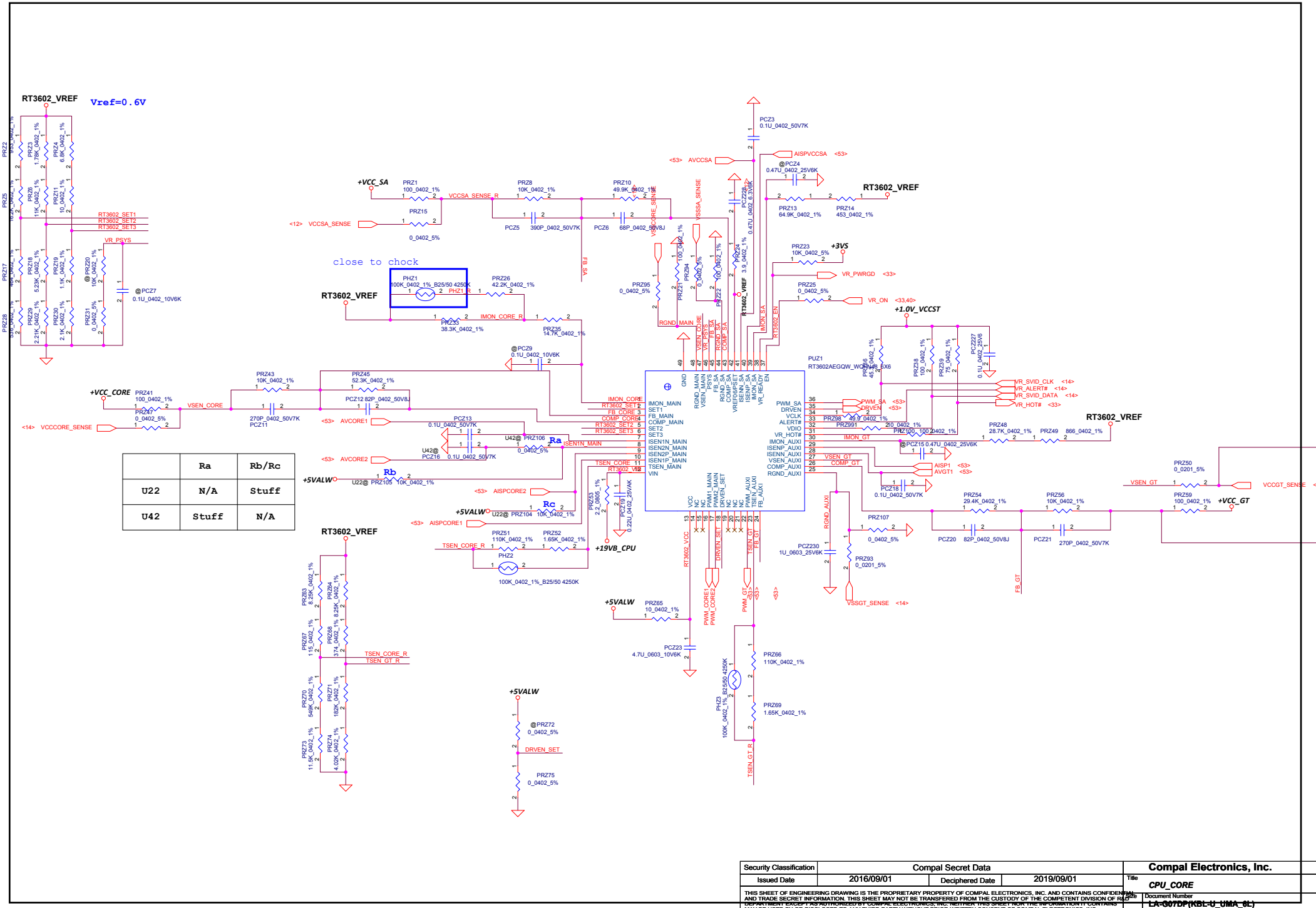

	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date 2019/09/01	Title: CPU_CORE

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	LA-G07DP(KBL-U_UMA_8L)		V0.3
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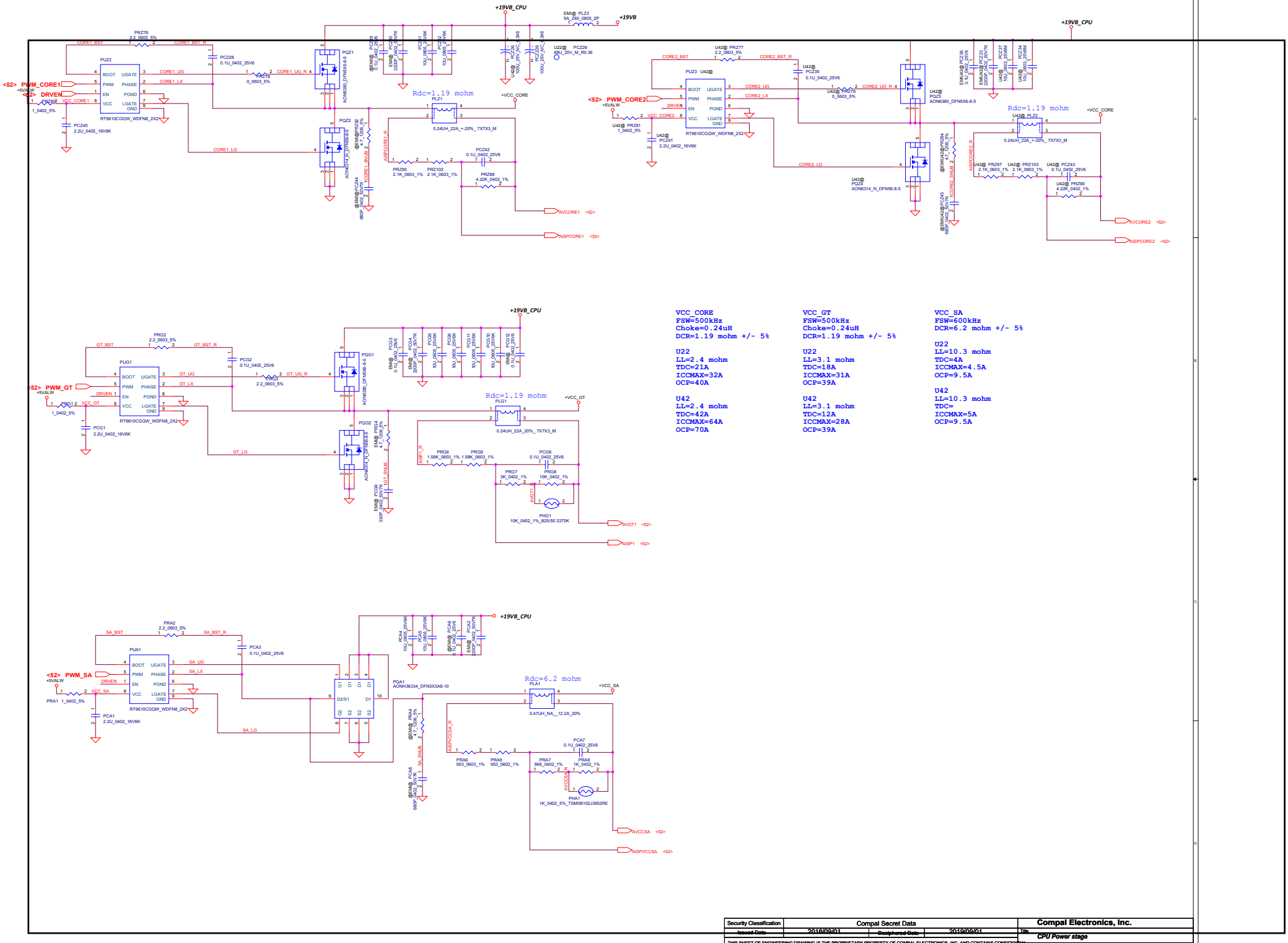

VCC_CORE
FSW=500kHz
Choke=0.24uH
DCR=1.19 mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC_GT
FSW=500kHz
Choke=0.24uH
DCR=1.19 mohm +/- 5%

U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

U42
LL=3.1 mohm
TDC=12A
ICCMAX=28A
OCP=39A

VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

U42
LL=10.3 mohm
TDC=
ICCMAX=5A
OCP=9.5A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01	Title: CPU Power stage

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+VCC_CORE

2016.12.29

VCC_CORE :
U22
390uF*1
22uF*18
1uF*35

U42
390uF*2
22uF*22
1uF*35

+VCC_GT

VCC_GT :
U22 & U42
390uF*1
22uF*33
1uF*13

+VCC_SA

VCC_SA :
U22 & U42
22uF*9
1uF*7

2016.11.21

2016.11.10

BOM option
by JU22(for GT) and JU42A (for IA)

U42@

+VCC_GT_VR

+VCC_GTX_VR

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01
Title	PROCESSOR DECOUPLING		
Size	Document Number		Rev
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Compal Electronics, Inc.

Title

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Security Classification	Compal Secret Data		
Issued Date	2015/09/01	Deciphered Date	2018/09/01

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Compal Electronics, Inc.

Title

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Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2018/09/01

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Compal Electronics, Inc.

Title

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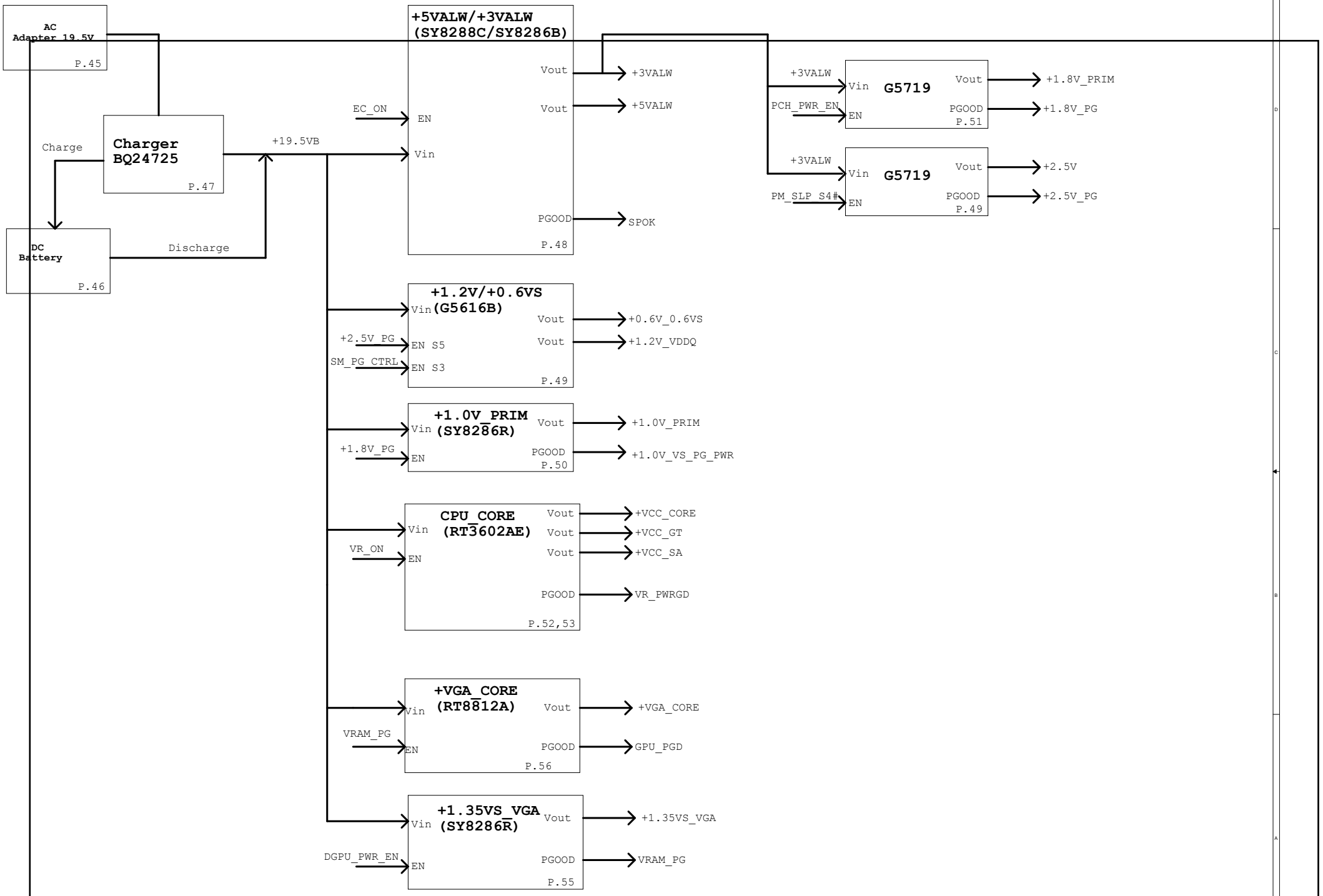

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Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Compal Electronics, Inc.

Title: *Power Block Diagram*

Size: B | Document Number: LA-G07DP(KBL-U_UMA_6L) | Rev: V0.3

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Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: <Path Name>

Size: C | Document Number: LA-G07DP(KBL-U_UMA_6L) | Rev: v0.3

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